L Number	Hits	Search Text	DB	Time stamp
1	157	substrate$1 same IC same (conductive near2 element$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:22
8	18	compress$3 same (substrate$1 same IC same (conductive near2 element$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 15:55
15	3	crystal$1 same (compress$3 same (substrate$1 same IC same (conductive near2 element$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 15:59
22	254523	257/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:00
29	66	257/$.ccls. and (substrate$1 same IC same (conductive near2 element$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:01
36	10	(compress$3 same (substrate$1 same IC same (conductive near2 element$1))) and (257/$.ccls. and (substrate$1 same IC same (conductive near2 element$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:01
43	17	(conductive near2 element$1) same compress$3 same crystal$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:22
50	17	(conductive near2 element$1) same compress$4 same crystal$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:23
57	4	(connector$1 or socket$1) same ((conductive near2 element$1) same compress$4 same crystal$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:24

L Number	Hits	Search Text	DB	Time stamp
1	157	substrate$1 same IC same (conductive near2 element$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:22
8	18	compress$3 same (substrate$1 same IC same (conductive near2 element$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:04
15	3	crystal$1 same (compress$3 same (substrate$1 same IC same (conductive near2 element$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 15:59
22	254523	257/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:00
29	66	257/$.ccls. and (substrate$1 same IC same (conductive near2 element$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:01
36	10	(compress$3 same (substrate$1 same IC same (conductive near2 element$1))) and (257/$.ccls. and (substrate$1 same IC same (conductive near2 element$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:01
43	17	(conductive near2 element$1) same compress$3 same crystal$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:22
50	17	(conductive near2 element$1) same compress$4 same crystal$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:23
57	4	(connector$1 or socket$1) same ((conductive near2 element$1) same compress$4 same crystal$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:28
64	60	mount$3 same (substrate$1 same IC same (conductive near2 element$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:29
71	13	(insulat$3) same (mount$3 same (substrate$1 same IC same (conductive near2 element$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:59
78	498	257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:59
85	5	(substrate$1 same IC same (conductive near2 element$1)) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:59
92	6	(compress$4 same connect$4 same IC$1) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:12

99	8	(compress$4 same substrate$1 same IC$1) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:20
106	108	(compress$4 same substrate$1) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:21
113	16	(compress$4 same substrate$1 same (IC$1 or (integrate$1 adj circuit$5))) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:25
120	2	5821763.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:26

L Number	Hits	Search Text	DB	Time stamp
1	157	substrate$1 same IC same (conductive near2 element$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:22
8	18	compress$3 same (substrate$1 same IC same (conductive near2 element$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:04
15	3	crystal$1 same (compress$3 same (substrate$1 same IC same (conductive near2 element$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 15:59
22	254523	257/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:00
29	66	257/$.ccls. and (substrate$1 same IC same (conductive near2 element$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:01
36	10	(compress$3 same (substrate$1 same IC same (conductive near2 element$1))) and (257/$.ccls. and (substrate$1 same IC same (conductive near2 element$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:01
43	17	(conductive near2 element$1) same compress$3 same crystal$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:22
50	17	(conductive near2 element$1) same compress$4 same crystal$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:23
57	4	(connector$1 or socket$1) same ((conductive near2 element$1) same compress$4 same crystal$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:28
64	60	mount$3 same (substrate$1 same IC same (conductive near2 element$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:29
71	13	(insulat$3) same (mount$3 same (substrate$1 same IC same (conductive near2 element$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:59
78	498	257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:59
85	5	(substrate$1 same IC same (conductive near2 element$1)) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 16:59
92	6	(compress$4 same connect$4 same IC$1) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:12

09/726,629

99	8	(compress$4 same substrate$1 same IC$1) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:20
106	108	(compress$4 same substrate$1) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:21
113	16	(compress$4 same substrate$1 same (IC$1 or (integrate$1 adj circuit$5))) and 257/E23.078.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:25
120	2	5821763.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:38
127	1715	bus same (process$3 or (CPU)) same (display$1 or lcd$1) same (IC$1 or (integrate$1 adj circuit$5))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:42
134	55	257/$.ccls. and (bus same (process$3 or (CPU)) same (display$1 or lcd$1) same (IC$1 or (integrate$1 adj circuit$5)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:42
141	0	257/E23.078.ccls. and (bus same (process$3 or (CPU)) same (display$1 or lcd$1) same (IC$1 or (integrate$1 adj circuit$5)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/24 17:42

	Document ID	Issue Date	Title	Current OR	Current XRef
1	US 20020171591	20021121	Ball grid array antenna	343/702	343/793; 343/895
2	US 20020071085 A1	20020613	Method for interconnecting a flat panel display having a non-transparent substrate and devices formed	349/149	
3	US 20020065965 A1	20020530	Solderless electronics packaging and methods of manufacture	710/100	257/E23.063; 257/E23.067; 257/E23.072; 257/E23.092; 257/E23.19; 257/E23.193
4	US 6556268 B1	20030429	Method for forming compact LCD packages and devices formed in which first bonding PCB to LCD panel and second bonding driver chip to PCB	349/149	349/151; 349/152
5	US 6537854 B1	20030325	Method for bonding IC chips having multi-layered bumps with corrugated surfaces and devices formed	438/118	257/737; 257/778; 438/612; 438/613
6	US 6501525 B2	20021231	Method for interconnecting a flat panel display having a non-transparent substrate and devices formed	349/150	379/149; 379/152
7	US 6373545 B1	20020416	Repairable TFT-LCD assembly and method for making in which a separation tape positioned between two anisotropic conductive	349/149	349/152
8	US 6362525 B1	20020326	Circuit structure including a passive element formed within a grid array substrate and method for making the same	257/738	257/528; 257/531; 257/668; 257/700; 257/701; 257/723; 257/728; 257/737; 257/777; 257/778; 257/E23.07; 361/760; 361/764; 361/765; 361/767; 438/238; 438/381
9	US 6348142 B1	20020219	Electroplating multi-trace circuit board substrates using single tie bar	205/125	205/163; 205/165; 205/167; 257/E23.06
10	JP 03116797 A	19910517	THICK FILM SURFACE PACKAGE CIRCUIT		174/256
11	EP 414378 A2	19910227	An adapter for integrated circuit elements and a method using the adapter for testing assembled		324/158.1
12	NN82035075	19820301	High Resolution Matrix Print Element Structure and Method For Manufacturing The Structure. March 1982.		

	Document ID	Issue Date	Title	Current OR	Current XRef
13	JP 2000068425 A	20000303	Mounting mechanism of IC chip, has electrically conductive element to connect wiring pattern formed on insulated substrate and chip electrode where copper board is attached to under surface of substrate		

US-PAT-NO: 6204089

DOCUMENT-IDENTIFIER: US 6204089 B1

TITLE: Method for forming flip chip package utilizing cone shaped bumps

DATE-ISSUED: March 20, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wang; Tsung-Hsiung	Taichung	N/A	N/A	TW

US-CL-CURRENT: 438/108, 257/E21.503 , 257/E21.508 , 257/E23.021

ABSTRACT:

A method for forming a flip chip package by using cone-shaped solder bumps and a package formed by such method are disclosed. In the method, an integrated circuit chip is first provided with a plurality of cone-shaped solder bumps formed on a plurality of bond pads. The cone-shaped solder bumps are equipped with sharp-pointed tip portions such that they penetrate an electrically insulating material layer that is positioned between the solder bumps on the IC chip and a substrate to be bonded thereto. When a lamination process is conducted on the IC chip and the substrate with the electrically insulating material layer thereinbetween, electrical communication between the plurality of bond pads and a plurality of conductive elements on the surface of the substrate is established when the cone-shaped solder bumps penetrate the electrically insulating material layer and form ohmic contact with the conductive elements on the substrate. The present invention novel method therefore eliminates many processing steps that are required in a conventional flip chip bonding process and provides an improved method that saves both costs and time.

14 Claims, 10 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

---------- KWIC ---------

Detailed Description Text - DETX (6):

A more detailed process flow for the present invention novel method is shown in FIG. 3. In the first process step 50, an **IC** chip that has an active surface and a plurality of bond pads formed of copper or aluminum is first provided. In the next process step, shown as step 52 in FIG. 3, a special bump preparation process is conducted which can be a direct-on-pad bump forming process or a transfer molding process that were previously described. The other major component used in the bonding process, ie. the **substrate** 54 which may be suitably a printed circuit board, a liquid **crystal** display structure or any other **substrates that has conductive elements, or conductive** traces formed thereon. When conductive traces of solder material is utilized, a surface finish step 54 may be required for pre-treating the solder surface with a wetting layer such as that shown in step 56. The prepared **substrate** and the prepared **IC** chip are then positioned in a fixture that is capable of applying a **compressive** force thereon and for aligning the chip and the **substrate** such that

the plurality of cone-shaped solder bumps are aligned with the plurality of **conductive elements** on the surface of the **substrate**. This is shown in step 60.

US-PAT-NO: 4763041

DOCUMENT-IDENTIFIER: US 4763041 A

TITLE: Dot array fluorescent tube for writing optical information in optical printer

DATE-ISSUED: August 9, 1988

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Segawa; Hideo	Tokyo	N/A	N/A	JP

US-CL-CURRENT: 313/496, 313/497 , 340/815.73 , 347/122 , 355/67

ABSTRACT:

A dot array fluorescent tube for an optical printer writes optical information on a photoconductive element by converting an information signal representative of a desired image to optical information. A grid electrode disposed in a vacuum space defined in a housing has a slot-like opening in a portion thereof which faces an array of fluorescent elements which are formed on anodes, which are also arranged in an array in the lengthwise direction of the housing. The grid electrode is formed as a metal film on the housing through an insulating layer. A conductive light intercepting film is deposited on the housing except for a limited portion which faces the fluorescent element array, thereby regulating the direction of light which is transmitted through the housing. The fluorescent elements in the array provide a plurality of dot arrays which are controlled independently of each other. Lead terminals are connected with the anodes and led out to the outside of the housing to be connected to external drive devices by an anisotropic conductive rubber connector. The lead terminals are divided into groups each made up of a predetermined number.

11 Claims, 18 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 8

---------- KWIC ---------

Detailed Description Text - DETX (24):

As shown in FIGS. 18 and 19, connection of the terminals L.sub.i on the **substrate** 112 and the electrode 144 on the **IC substrate** 142 is accomplished by fastening retainer plates 152 and 154 to each other by screws 156 with an anisotropic conductive rubber connector 150. As shown in FIG. 19, the anisotropic conductive rubber connector 150 comprises **conductive elements** 160 arranged in a mass of insulative rubber 158 in a predetermined direction and at predetermined pitches. The terminals L.sub.i and 144 can be readily and surely interconnected merely by **compressing** the connector 150 therebetween. The connector 150 of the kind described, which has found applications such as to liquid **crystal** display panels, is capable of interconnecting terminals at pitches up to 200 microns. Therefore, it is sufficiently applicable even to an optical printer if, in the case of a ten terminals per millimeter arranement, for example, the lead terminals L.sub.i are distributed in the alternating manner as shown in FIG. 3, i.e., at pitches of 200 microns. The **IC substrate**

142 may be made of a flexible material such as polyimide in order to arrange the **IC** chips 140 on the back of the **substrate** 12 and, thereby, render the whole configuration compact. Furthermore, in accordance with this embodiment, the **substrate** 12 even if made of glass will be prevented from being broken in contrast to the case of thermocompression bonding and, in addition, when any of the fluorescent elements 20.sub.i or the like on the **substrate** 12 has failed, it is needless to replace the comparatively expensive ICs 140 and only the **substrate** 12 should be replaced. As described above, this particular embodiment accomplishes the fifth object of the present invention.

US-PAT-NO: 6537854

DOCUMENT-IDENTIFIER: US 6537854 B1

TITLE: Method for bonding IC chips having multi-layered bumps with corrugated surfaces and devices formed

DATE-ISSUED: March 25, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chang; Shyh-Ming	Hsinchu	N/A	N/A	TW
Jou; Jwo-Huei	Hsin-chu	N/A	N/A	TW
Wu; Chi-Yuan	Hsinchu	N/A	N/A	TW

US-CL-CURRENT: 438/118, **257/737** , **257/778** , 438/612 , 438/613

ABSTRACT:

A method for bonding an **IC** chip formed with corrugated, multi-layered bumps to **conductive elements on a substrate** and devices formed by such method are disclosed. In the method, multi-layered bumps are formed by a cover layer of a conductive metal deposited on a base layer of a compliant material. The exposed bonding surface of the bump is formed in a corrugated fashion, or in a serrated shape with saw-tooth configurations. The saw-tooth configurations may either be rectangular or triangular. In the bonding method, instead of using an anisotropic conductive film loaded with conductive particles, a solid adhesive film without conductive particles or a liquid adhesive material without conductive particles can be utilized. The serrated bonding surface of the bumps is effective in expelling the adhesive material from the bonding interface between the bumps and the **conductive elements** such that a low resistance bond can be formed between an **IC** chip and a **substrate**. The solid adhesive layer or the liquid adhesive material, after bonding and curing, functions effectively as a moisture barrier layer.

23 Claims, 14 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

---------- KWIC ---------

Abstract Text - ABTX (1):

A method for bonding an **IC** chip formed with corrugated, multi-layered bumps to **conductive elements on a substrate** and devices formed by such method are disclosed. In the method, multi-layered bumps are formed by a cover layer of a conductive metal deposited on a base layer of a compliant material. The exposed bonding surface of the bump is formed in a corrugated fashion, or in a serrated shape with saw-tooth configurations. The saw-tooth configurations may either be rectangular or triangular. In the bonding method, instead of using an anisotropic conductive film loaded with conductive particles, a solid adhesive film without conductive particles or a liquid adhesive material without conductive particles can be utilized. The serrated bonding surface of the bumps is effective in expelling the adhesive material from the bonding interface between the bumps and the **conductive elements** such that a low resistance bond can be formed between an **IC** chip and a **substrate**. The solid

adhesive layer or the liquid adhesive material, after bonding and curing, functions effectively as a moisture barrier layer.

Brief Summary Text - BSTX (7):

In still another technique for bonding a LCD to a PCB, as shown in FIGS. 1A and 1B, a chip on glass (COG) technique is used. In the COG technique, an **IC** chip 12 can be mounted directly to a glass **substrate** 14 of an LCD by utilizing solder bumps 16 and an anisotropic conductive film (ACF) 18. The ACF tape 18 contains electrically conductive particles 20 which are embedded in an insulative material 22. Positioned under the ACF 18 is the LCD **substrate** 14 which has **conductive elements** 24 formed on top. After the **IC** chip 12, the ACF 18 and the LCD **substrate** 14 are pressed together under heat, as shown in FIG. 1B, the conductive particles 20 provides electrical communication between the solder bumps 16 and the **conductive elements** 24 and therefore allowing the **IC** chip 12 to electrically communicate with the LCD **substrate** 14, i.e., the **IC** chip 12 may be a driver chip which is connected to the drive lines on the LCD. It should be noted that, electrical communication between the solder bumps 16 and the **conductive elements** 24 is only established where the conductive particles 20 are **compressed,** i.e., only established anisotropically and selectively. The **conductive elements** 24 on the LCD **substrate** 10 is normally formed of indium-tin-oxide (ITO) thin films.

Brief Summary Text - BSTX (9):

The traditional COG technique shown in FIGS. 1A and 1B may be carried out in an alternate method of using a liquid adhesive. This is shown in FIGS. 2A and 2B. In this alternate COG technique, an **IC** chip 12 is mounted directly to a glass **substrate** 14 of an LCD by solder bumps 16 and a liquid adhesive 26. The liquid adhesive 26 can be suitably an acrylic or an epoxy which can be cured by either an UV light or by heat. The liquid adhesive 26 can be dispensed in droplets such as shown in FIG. 2A on top of the glass **substrate** 14 over the **conductive elements** 24 formed on the **substrate**. The **conductive elements** 24 may be suitably formed of a conductive film such as ITO. After the liquid adhesive 26 is dispensed on the top surface 28 of the glass **substrate** 14, the **IC** chip 12 may be pressed onto the **substrate** 14 under a suitable pressure and heated to a suitable temperature. The pressure exerted enables the **conductive elements** 24 to intimately contact the solder bumps 16 such that an ohmic bond is formed thereinbetween. The liquid adhesive 26 fills the gap between the **conductive elements** 24 or the solder bumps 16 and solidifies after the curing process. The solidified liquid adhesive 26 functions as a stress buffer and a moisture barrier for protecting the bond formed between the **conductive elements** 24 and the solder bumps 16 from stress fracture or moisture attack. The bonded structure is shown in FIG. 2B.

Brief Summary Text - BSTX (14):

It is therefore an object of the present invention to provide a method for bonding an **IC** chip equipped with solder bumps to **conductive elements on a substrate** that does not have the drawbacks and shortcomings of the conventional bonding methods.

Brief Summary Text - BSTX (15):

It is another object of the present invention to provide a method for bonding an **IC** chip equipped with solder bumps to **conductive elements on a substrate** that does not require the use of an anisotropic conductive film thereinbetween.

Brief Summary Text - BSTX (16):

It is a further object of the present invention to provide a method for bonding an **IC** chip equipped with solder bumps to **conductive elements on a**

substrate that does not require the use of an liquid adhesive as an underfill material thereinbetween.

Brief Summary Text - BSTX (17):
It is another further object of the present invention to provide a method for bonding an IC chip equipped with solder bumps to conductive elements on a substrate wherein the bumps are formed in a multi-layer structure.

Brief Summary Text - BSTX (18):
It is still another object of the present invention to provide a method for bonding an IC chip equipped with solder bumps to conductive elements on a substrate wherein the solder bumps are formed by a compliant material coated with an electrically conductive metal.

Brief Summary Text - BSTX (19):
It is yet another object of the present invention to provide a method for bonding an IC chip equipped with solder bumps to conductive elements on a substrate wherein the bumps are formed in a multi-layered structure having a corrugated contact surface.

Brief Summary Text - BSTX (23):
In accordance with the present invention, a method for bonding an IC chip that has corrugated multi-layered bumps to conductive elements on a substrate and devices formed by the method are provided.

Brief Summary Text - BSTX (24):
In a preferred embodiment, a method for bonding an IC chip that has corrugated multi-layered bumps to a substrate can be carried out by the steps of providing an IC chip that has an active surface equipped with multi-layered bumps, the multi-layered bumps include a base layer which is formed of a compliant material and a cover layer which is formed of a conductive metal, the cover layer is in electrical communication with input/output pads on which the bumps are built, the multi-layered bumps are formed in a corrugated shape with outwardly protruding chips, providing a substrate that has a top surface equipped with conductive elements that are positioned corresponding to the bumps on the IC chip, positioning an electrically insulative, stress-buffering material between the conductive elements and the bumps, and compressing and heating the IC chip and the substrate together with the bumps contacting the conductive elements through the electrically insulative, stress-buffering material until electrical communication between the outwardly protruding chips on the bumps and the conductive elements are established.

Detailed Description Text - DETX (2):
The present invention provides a method for bonding an IC chip that is equipped with corrugated, multi-layered bumps to conductive elements on a substrate and devices formed by such method. In the method, an IC chip is provided which has an active surface built with corrugated multi-layered bumps constructed by a base layer of a compliant material and a cover layer of a conductive metal. The cover layer of the bumps is in electrical communication with an input/output pad the bump is built on. The corrugated multi-layered bump is formed with a corrugated surface which has outwardly protruding tips for making contact with conductive elements on a substrate.

Detailed Description Text - DETX (3):
Instead of utilizing an anisotropic conductive film layer for providing electrical communication between bumps on an IC chip and conductive elements on

a substrate, a solid adhesive film or a liquid adhesive material is utilized. The corrugated bonding surface of a bump penetrates the solid adhesive film or the liquid adhesive layer to make an ohmic contact with a conductive element on the substrate establishing electrical communication. The performance and processing difficulties caused by the conductive particles in the anisotropic conductive film can be eliminated by the present invention novel method. Furthermore, the solid adhesive film or the liquid adhesive material can be utilized at a substantially lower cost than the ACF films. Since there are no conductive particles in the solid adhesive film and there is no chance for causing a short, a higher circuit density utilizing a pitch smaller than 50 .mu.m can be realized. Furthermore, the IC chip/substrate package can be utilized in high frequency applications since there are no conductive particles for causing radio frequency interferences.

Detailed Description Text - DETX (11):

In another application utilizing liquid adhesive, as shown in the present invention fourth preferred embodiment in FIGS. 6A and 6B, an IC chip 30 equipped with bumps 50 similar to that in the second preferred embodiment are used. The difference being that instead of the solid adhesive layer 32 (shown in FIG. 4A), a droplet 56 of a liquid adhesive is dispensed on the top surface 48 of the glass substrate 34. The serrated bonding surface 40 of the bump 50 is formed in separate columns each having a cover layer 42 of a conductive metal and a base layer 44 of a compliant material. The formation of the serrated bump 50 is similar to that shown in the second preferred embodiment of FIG. 4A. The serrated bonding surface 40 can be advantageously used to separate and push away the liquid adhesive material 56 during the bonding process when the IC chip 30 is compressed against the glass substrate 34 such that electrical communication between the bump 50 and the conductive element 24 can be established. It should be noted that the liquid adhesive material 56, after curing either by UV light or by heat, forms an underfill layer between the IC chip 30 and the glass substrate 34 for both stress-buffering and moisture-sealing functions. This is shown in FIG. 6B.

Detailed Description Text - DETX (13):

FIG. 7B shows a second implementation example of the present invention novel method in which a bump 70 is formed on the surface of the IC chip 58. The bump 70 is similar to that shown in the second and fourth preferred embodiment of the present invention method previously. Similar to the example shown in FIG. 7A, a cover layer of conductive material 72 is utilized to extend a bond pad 76 from a peripheral array to a bond pad 78 in an area array. An I/O redistribution is thus accomplished. The bump 70 is bonded to a conductive element 82 formed on a top surface 84 of a glass substrate 78.

Detailed Description Text - DETX (14):

The present invention novel method for forming corrugated, multi-layered bumps on the surface of an IC chip for bonding to conductive elements on a substrate and devices formed by such method have therefore been amply described in the above descriptions and in the appended drawings of FIGS. 3A.about.7B.

Claims Text - CLTX (1):

1. A method for bonding an IC chip having corrugated multi-layered bumps to a substrate comprising the steps of: providing an IC chip having an active surface equipped with multi-layered bumps, said multi-layered bumps comprising a base layer formed of a compliant material and a cover layer formed of a conductive metal, said cover layer being in electrical communication with input/output pads onto which said bumps are built, said multi-layered bumps being formed in a corrugated shape with outwardly protruding tips, providing a substrate having a top surface equipped with conductive elements positioned corresponds to said bumps on said IC chip, positioning a solid sheet of an

electrically insulative material between said **conductive elements** and said bumps, and **compressing** and heating said **IC** chip and said **substrate** together with said bumps contacting said **conductive elements** through said electrically insulative material until electrical communication between said outwardly protruding tips on said bumps and said **conductive elements** is established.

Current US Cross Reference Classification - CCXR (1):
257/737

Current US Cross Reference Classification - CCXR (2):
257/778

US-PAT-NO: 6336269

DOCUMENT-IDENTIFIER: US 6336269 B1

TITLE: Method of fabricating an interconnection element

DATE-ISSUED: January 8, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Eldridge; Benjamin N.	Hopewell Junction	NY	12533	N/A
Grube; Gary W.	Monroe	NY	10950	N/A
Khandros; Igor Y.	Peekskill	NY	10566	N/A
Mathieu; Gaetan L.	Carmel	NY	10512	N/A

US-CL-CURRENT: 29/885, 228/180.5 , 228/199 , **257/E21.503** , **257/E21.509** , **257/E21.511** , **257/E21.512** , **257/E21.519** , **257/E21.525** , **257/E23.021** , **257/E23.024** , **257/E23.068** , **257/E23.078** , **257/E25.011** , **257/E25.029** , 29/825 , 29/830 , 29/840 , 29/843

ABSTRACT:

Contact structures formed on an electronic component are useful for connecting the component to other electronic components. A contact tip structure can be formed on a sacrificial substrate, then combined with an interconnection element. A preferred contact structure includes some topography, generally in the form of certain raised features. These are formed by embossing depressed features into the sacrificial substrate upon which the contact tip structure is constructed. The contact tip structure can be optimized for making contact with another electrical component.

23 Claims, 177 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 60

---------- KWIC ---------

Brief Summary Text - BSTX (22):

One recent effort directed to making resilient connections is described in an article entitled ELASTOMERIC CONNECTOR FOR MCM AND TEST APPLICATIONS, ICEMM Proceedings, 1993, pages 341-346, which describes an "Elasticon" (tm) connector. The Elasticon connector uses solid gold or gold alloy wires for the **conductive elements,** embedded in an elastomer material (e.g., liquid elastomer resin injected into a mold cavity), and is generally targeted at the interconnection requirements for land grid array (LGA) packages for multichip (MCM) and single (SCM) chip modules. The size, shape and spacing of the wires, along with the elastomer material properties, can be tailored to specific application requirements which include MCM and SCM packaging, board-to-board and cable-to-board interconnections, as well as high density PCB and **IC** chip testing applications. The solid gold wires and the silicone elastomer material are impervious to corrosion. FIG. 1 of the article illustrates a basic embodiment of the Elasticon connector, wherein a plurality of wires are ball-bonded to a rigid **substrate** and extend straight at an angle (e.g., 45-85.degree.) from the surface of the **substrate**. Attachment of the proximal

ends of the wires to the **substrate** is by an angled flying lead wire bonding process using **compressive** force and ultrasonic energy applied through the capillary tip and thermal energy applied through the heated stage on the wirebonder. The capillary and **substrate** are positioned to allow a shear blade mechanism to sever the wire at the desired height and angle from the **substrate** surface. Electronic flame-off (EFO) is used to melt the wire extending from the capillary tip to start the next ball bond (of the proximal end of the next wire to be bonded to the **substrate**). After mounting all of the wires to the **substrate,** a ball-shaped contact is formed at the far (distal) end of each wire by a process of laser ball forming, and the plurality of wires are embedded in an elastomer material. The ball-shaped (enlarged) distal ends help prevent the wires from vibrating loose and causing shorts between contacts. As noted in the article, the angled orientation of the conductors is necessary to minimize plastic deformation of the wires as an Elasticon connector is **compressed** between two parallel surfaces. The angled orientation also provides a "wiping" contact surface which, when the connector is **compressed,** will cause the wires to rotate and slide against the mating contact surfaces. The article discusses the use of gold/palladium alloys and platinum for the wires. FIG. 3 of the article describes clustering wires in groups of one to four wires per contact, in conjunction with forming grooves in the elastomer between each group of wires. The various embodiments of the Elasticon connector described in the article require a **substrate** of ceramic, metal, silicon or epoxy-glass laminate material, and interposer embodiments require an etchable **substrate** material such as copper with a thin layer of gold on the top surface. FIG. 8 of the article describes integrated probe contacts and aptly notes that the ability to test for known good dies has been one of the stumbling blocks for MCM packaging. As shown therein, a probe matrix uses 2 mil (0.002 inch) diameter gold wires in an array. The probes can permanently be attached to the test module, or fabricated as an interposer structure. U.S. Pat. No. 5,386,344 (Beaman, et al.; January 1995; USCL 361/785), entitled FLEX CIRCUIT CARD ELASTOMERIC CABLE CONNECTOR ASSEMBLY, discloses a related "Elastipac" (tm) elastomeric cable connector.

Current US Cross Reference Classification - CCXR (3):
257/E21.503

Current US Cross Reference Classification - CCXR (4):
257/E21.509

Current US Cross Reference Classification - CCXR (5):
257/E21.511

Current US Cross Reference Classification - CCXR (6):
257/E21.512

Current US Cross Reference Classification - CCXR (7):
257/E21.519

Current US Cross Reference Classification - CCXR (8):
257/E21.525

Current US Cross Reference Classification - CCXR (9):
257/E23.021

Current US Cross Reference Classification - CCXR (10):

257/E23.024

Current US Cross Reference Classification - CCXR (11):
257/E23.068

Current US Cross Reference Classification - CCXR (12):
257/E23.078

Current US Cross Reference Classification - CCXR (13):
257/E25.011

Current US Cross Reference Classification - CCXR (14):
257/E25.029

US-PAT-NO: 6302702

DOCUMENT-IDENTIFIER: US 6302702 B1

TITLE: Connecting devices and method for interconnecting circuit components

DATE-ISSUED: October 16, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Audet; Gerald P.	Granby	N/A	N/A	CA
Guerin; Luc	Granby	N/A	N/A	CA
Landreville; Jean-Luc	Granby	N/A	N/A	CA

US-CL-CURRENT: 439/66, **257/E23.068** , 439/74

ABSTRACT:

An integrated circuit package having metallized contact pads is provided with electrically conducting devices permanently attached to each contact pad. The devices are flexed when so attached, and are aligned and assembled onto corresponding pads of a second electrical component (e.g., a printed circuit board) to provide electrical connection between the integrated circuit package and the second electrical component.

9 Claims, 8 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

---------- KWIC ---------

Brief Summary Text - BSTX (4):

In the mounting of an integrated circuit package to a printed board (PCB), or similar support **substrate,** there are different methods of providing electrical interconnections between the package's input/output (I/O) pads and the **substrate's** pads. One method of interconnection, referred to as land grid array interconnection, uses a land grid array socket. This socket comprises a plurality of compressible **conductive elements** placed between the **IC** package and the **substrate**.

Brief Summary Text - BSTX (5):

The compressible **conductive elements** are maintained in an array that corresponds to the package I/O pad array, by means of an electrically insulating matrix that acts as a contact support, or retainer. The land grid array socket is placed between the package and **substrate**. The **IC** package and **substrate** are held together with appropriate **compression** hardware, thereby causing each and every **conductive element to be compressed** and thus create appropriate contact force between its corresponding **IC** package pad and **substrate** pad, which ensures an electrically conductive path between those pads.

Brief Summary Text - BSTX (6):

An example of a land grid array socket is shown in U.S. Pat. No. 4,922,376 to Pommer et al, entitled "Spring Grid Array Interconnection for Active Microelectronic Elements" and issued May 1, 1990. This patent describes the use of a plurality of **conductive resilient elements,** held in an insulating contact retainer having a plurality of apertures to hold each **conductive element**. The resilient elements provide an electrical connection between pads of the **IC** package and those of a **substrate**.

Brief Summary Text - BSTX (12):

Another commonly used method for electrically connecting integrated circuit packages to **substrates** is known as surface mounting. For this type of connection, leads, solder balls, or any other solderable interconnection means are permanently attached to the **IC** package; which in turn are permanently attached to the printed circuit board pads by means of soldering. U.S. Pat. No. 4,751,199 to Phy, entitled "Process for Forming a Complaint Lead Frame for Array-type Semiconductor Packages", issued Jun. 14, 1998, shows one example of a surface mountable component, with discrete complaint **conductive elements** suitable for surface attachment to the printed circuit board by conventional surface mount assembly soldering.

Current US Cross Reference Classification - CCXR (1):

257/E23.068

US-PAT-NO: 6204089

DOCUMENT-IDENTIFIER: US 6204089 B1

TITLE: Method for forming flip chip package utilizing cone shaped bumps

DATE-ISSUED: March 20, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wang; Tsung-Hsiung	Taichung	N/A	N/A	TW

US-CL-CURRENT: 438/108, **257/E21.503** , **257/E21.508** , **257/E23.021**

ABSTRACT:

A method for forming a flip chip package by using cone-shaped solder bumps and a package formed by such method are disclosed. In the method, an integrated circuit chip is first provided with a plurality of cone-shaped solder bumps formed on a plurality of bond pads. The cone-shaped solder bumps are equipped with sharp-pointed tip portions such that they penetrate an electrically insulating material layer that is positioned between the solder bumps on the **IC** chip and a **substrate** to be bonded thereto. When a lamination process is conducted on the **IC** chip and the **substrate** with the electrically insulating material layer thereinbetween, electrical communication between the plurality of bond pads and a plurality of **conductive elements** on the surface of the **substrate** is established when the cone-shaped solder bumps penetrate the electrically insulating material layer and form ohmic contact with the **conductive elements on the substrate**. The present invention novel method therefore eliminates many processing steps that are required in a conventional flip chip bonding process and provides an improved method that saves both costs and time.

14 Claims, 10 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

---------- KWIC ---------

Abstract Text - ABTX (1):

A method for forming a flip chip package by using cone-shaped solder bumps and a package formed by such method are disclosed. In the method, an integrated circuit chip is first provided with a plurality of cone-shaped solder bumps formed on a plurality of bond pads. The cone-shaped solder bumps are equipped with sharp-pointed tip portions such that they penetrate an electrically insulating material layer that is positioned between the solder bumps on the **IC** chip and a **substrate** to be bonded thereto. When a lamination process is conducted on the **IC** chip and the **substrate** with the electrically insulating material layer thereinbetween, electrical communication between the plurality of bond pads and a plurality of **conductive elements** on the surface of the **substrate** is established when the cone-shaped solder bumps penetrate the electrically insulating material layer and form ohmic contact with the **conductive elements on the substrate**. The present invention novel method therefore eliminates many processing steps that are required in a conventional

flip chip bonding process and provides an improved method that saves both costs and time.

Brief Summary Text - BSTX (11):

The conventional method for depositing solder bumps described above presents a number of processing difficulties. For instance, one of the difficulties is the large volume of solder used in a mushroom-shaped bump which impedes the process of making fine-pitched bumps. The other processing difficulties are the complexity of the method and the large number of processing steps required. For instance, FIG. 2 illustrates, on the left side of the figure, the processing steps required for a conventional flip chip bonding method. First, the **IC** chip is prepared by forming aluminum bond pad on the chip, followed by an under-bump-metallurgy (UBM) process for preparing bonding sites for solder bumps, and then the solder bumping or bump forming process by electrodeposition, electroless deposition, etc. The **substrate** must also be prepared by coating a flux coating layer on top of the **conductive elements** that the solder bumps are bonded to. The flip chip bonding process is then carried out by pressing the solder bumps on the **IC** chip against the **conductive elements on the substrate** together forming bonds, the solder bumps are then reflown to ensure ohmic contacts are established between the solder bump and the **conductive elements**. The solder bumps on the **IC** chip may optionally be coated with a flux coating layer by a fluxer (or a doctor plane). A flux cleaning step is then required to remove the excess flux coating on the **substrate** followed by a drying step for removing the cleaning solvent. In the final steps of the flip chip bonding process, an underfill material is used to fill the gaps between the **IC** chip and the **substrate** for passivation and for relieving thermal stresses, followed by a curing or annealing process for the underfill layer. As shown in FIG. 2, there are at least ten major processing steps required in the conventional flip chip bonding method to complete a flip chip package.

Brief Summary Text - BSTX (16):

It is still another object of the present invention to provide a method for forming a flip chip package by utilizing cone-shaped solder bumps provided on an **IC** chip and heating an electrically insulating material layer positioned in-between the **IC** chip and a **substrate** to a temperature of at least 150.degree. C. for bonding the solder bumps to the **conductive elements on the substrate**.

Brief Summary Text - BSTX (17):

It is yet another object of the present invention to provide a method for forming a flip chip package by using cone-shaped solder bumps on an **IC** chip and a dielectric material layer having a thickness between about 10 .mu.m and about 250 .mu.m between the **IC** chip and a **substrate** wherein the solder bumps penetrate the dielectric material layer establishing electrical communication with **conductive elements on the substrate**.

Brief Summary Text - BSTX (22):

In a preferred embodiment, a method for forming a flip chip package by using cone-shaped solder bumps can be carried out by the steps of first providing an integrated circuit chip equipped with a first plurality of bond pads on an active surface, building a first plurality of cone-shaped bumps on the first plurality of bond pads, providing a **substrate** that has a second plurality of **conductive elements** formed on a top surface, positioning an electrically insulating material layer on the top surface of the **substrate, and compressing the IC** chip and the **substrate** together with the electrically insulating material layer thereinbetween at a temperature of at least 150.degree. C. such that electrical communication is established between the first plurality of bond pads and the second plurality of **conductive elements** when the first plurality of cone-shaped bumps penetrates the electrically insulating material

layer and contacts the second plurality of **conductive elements**.

Brief Summary Text - BSTX (25):

The present invention is further directed to a flip chip package that is formed by cone-shaped solder bumps which includes an **IC** chip that is equipped with a first plurality of bond pads on an active surface and a first plurality of cone-shaped bumps on the bond pads, a **substrate** that has a second plurality of **conductive elements** on a top surface, and an electrically insulating material layer bonding the **IC** chip and the **substrate** together wherein the first plurality of cone-shaped bumps penetrates the electrically insulating material layer such that the first plurality of bond pads is in electrical communication with the second plurality of **conductive elements** through the cone-shaped bumps.

Brief Summary Text - BSTX (26):

In the flip chip package that is formed by cone-shaped solder bumps, the **IC** chip is a flip chip and the **substrate** is a printed circuit board or a liquid crystal display **substrate**. The electrically insulating material layer may be formed of a dielectric material, such as a polymeric-based adhesive material. The electrically insulating material layer may be a laminate with an electrically insulating core layer sandwiched between two layers of electrically insulating adhesive material, wherein the core layer may be formed of a liquid crystal polymer, a polyimide, an epoxy or a polyaramid, and the electrically insulating adhesive material may be formed of an epoxy, a polyimide or a polyester. The electrically insulating material layer may be formed of a thickness of between about 10 .mu.m and about 250 .mu.m, and may have a glass transition temperature between about 150.degree. C. and about 300.degree. C. The second plurality of **conductive elements provided on the substrate** may be conductive traces formed of an electrically conductive metal.

Detailed Description Text - DETX (6):

A more detailed process flow for the present invention novel method is shown in FIG. 3. In the first process step 50, an **IC** chip that has an active surface and a plurality of bond pads formed of copper or aluminum is first provided. In the next process step, shown as step 52 in FIG. 3, a special bump preparation process is conducted which can be a direct-on-pad bump forming process or a transfer molding process that were previously described. The other major component used in the bonding process, ie. the **substrate** 54 which may be suitably a printed circuit board, a liquid crystal display structure or any other **substrates that has conductive elements, or conductive** traces formed thereon. When conductive traces of solder material is utilized, a surface finish step 54 may be required for pre-treating the solder surface with a wetting layer such as that shown in step 56. The prepared **substrate** and the prepared **IC** chip are then positioned in a fixture that is capable of applying a **compressive** force thereon and for aligning the chip and the **substrate** such that the plurality of cone-shaped solder bumps are aligned with the plurality of **conductive elements** on the surface of the **substrate**. This is shown in step 60.

Detailed Description Text - DETX (7):

In-between the **IC** chip and the **substrate,** an adhesive layer, as shown in step 62, of a dielectric nature is positioned. A lamination process under a suitable pressure and a suitable temperature, such as shown in step 64, is then carried out. It has been found that when an adhesive layer, or an electrically insulating material layer having a thickness between about 15 mm and about 250 .mu.m is utilized, the desirable lamination condition used may be a temperature between about 150.degree. C. and about 300.degree. C., and a pressure between about 50 psi and about 200 psi. In the last step 66 of the process, the solder bumps are reflown at an elevated temperature, such as a temperature of at least 180.degree. C. and the solder connections between the bond pads and the **conductive elements** are post-cured to improve bond strength and relieve thermal

stresses.

Detailed Description Text - DETX (10):
The **substrate** 74 provided for bonding to the **IC** chip 70 in the flip chip package may be suitably a printed circuit board, a liquid crystal display structure or any other suitable **substrate**. On a top surface 88 of the **substrate** 74, a second plurality of **conductive elements** 90 are provided. The **conductive elements** 90 may be in a form of conductive traces that are formed by an electrically conductive metal. The **conductive elements** 90 may further be provided in the form of bond pads on a printed circuit board.

Current US Cross Reference Classification - CCXR (1):
257/E21.503

Current US Cross Reference Classification - CCXR (2):
257/E21.508

Current US Cross Reference Classification - CCXR (3):
257/E23.021

US-PAT-NO: 5199889

DOCUMENT-IDENTIFIER: US 5199889 A

TITLE: Leadless grid array socket

DATE-ISSUED: April 6, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
McDevitt, Jr.; John E.	Cumberland	RI	N/A	N/A

US-CL-CURRENT: 439/66, 29/843 , 439/71 , 439/885

ABSTRACT:

An interconnection system for connecting leadless grid arrays of integrated circuits with leadless grid arrays of printed circuit boards. The system includes an insulative socket, flexible conductive elements and a compression lid. The insulative socket is temporarily affixed to the printed circuit board as the conductive elements, retained on a flexible carrier, are inserted into cavities of the socket. The cavities of the socket have inside dimensions greater than the outside dimensions of the conductive elements. After the conductive elements have been affixed to the printed circuit board, the flexible carrier is taken off of the elements and the insulative socket may be removed for visual inspection of the connection between the contact pads of the circuit board and the conductive elements. The integrated circuit is placed on top of the conductive elements such that contact pads of the circuit are properly aligned with appropriate contact pads of the printed circuit board. The compression lid is placed over the integrated circuit and affixed to the printed circuit board so as to secure the contact pads of the integrated circuit to the conductive elements.

20 Claims, 15 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

---------- KWIC ---------

Detailed Description Text - DETX (2):

As illustrated in FIGS. 1-4, an interconnection system 1 of the present invention preferably comprises a socket insulator 2, a **conductive element** 3 and a **compression** lid 4. The combination of components comprising said interconnection system 1 is used in conjunction with a PCB 5 and an IC 6, wherein said IC 6 comprises a plurality of IC contact pads 7 forming a leadless grid contact array. Said socket insulator 2 comprises a plurality of socket cavities 8, as illustrated in FIG. 2. Said socket insulator 2 is preferably molded of a liquid **crystal** polymer, or similar high-temperature thermoset resin compound, of the type generally used in the field as a fine-line molding material. Said socket cavities 8 are formed such that they are aligned with PCB contact pads 9. Said socket insulator 2 is temporarily retained on said PCB 5 by a plurality of insulator retention legs 17. Said retention legs 17 may be formed of the same material used in making said socket insulator 2. Furthermore, in the preferred embodiment, said retention legs 17 and said socket insulator 2 are fabricated as one piece. Retention ribs 11 of said

retention legs 17 provide the locking means by which said socket insulator 2 is temporarily retained on said PCB 5. In use, said retention legs 17 are inserted into retention cavities 18 located along the perimeter of said PCB 5 and locked into place with said retention ribs 11. Said retention legs 17 may vary in length in accordance with the size of said PCB 5 and whether a plurality of circuit boards are to be stacked together, as illustrated in FIG. 1A.

US-PAT-NO: 5199889

DOCUMENT-IDENTIFIER: US 5199889 A

TITLE: Leadless grid array socket

DATE-ISSUED: April 6, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
McDevitt, Jr.; John E.	Cumberland	RI	N/A	N/A

US-CL-CURRENT: 439/66, 29/843 , 439/71 , 439/885

ABSTRACT:

An interconnection system for connecting leadless grid arrays of integrated circuits with leadless grid arrays of printed circuit boards. The system includes an insulative socket, flexible conductive elements and a compression lid. The insulative socket is temporarily affixed to the printed circuit board as the conductive elements, retained on a flexible carrier, are inserted into cavities of the socket. The cavities of the socket have inside dimensions greater than the outside dimensions of the conductive elements. After the conductive elements have been affixed to the printed circuit board, the flexible carrier is taken off of the elements and the insulative socket may be removed for visual inspection of the connection between the contact pads of the circuit board and the conductive elements. The integrated circuit is placed on top of the conductive elements such that contact pads of the circuit are properly aligned with appropriate contact pads of the printed circuit board. The compression lid is placed over the integrated circuit and affixed to the printed circuit board so as to secure the contact pads of the integrated circuit to the conductive elements.

20 Claims, 15 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

---------- KWIC ---------

Detailed Description Text - DETX (2):

As illustrated in FIGS. 1-4, an interconnection system 1 of the present invention preferably comprises a **socket** insulator 2, a **conductive element** 3 and a **compression** lid 4. The combination of components comprising said interconnection system 1 is used in conjunction with a PCB 5 and an IC 6, wherein said IC 6 comprises a plurality of IC contact pads 7 forming a leadless grid contact array. Said **socket** insulator 2 comprises a plurality of **socket** cavities 8, as illustrated in FIG. 2. Said **socket** insulator 2 is preferably molded of a liquid **crystal** polymer, or similar high-temperature thermoset resin compound, of the type generally used in the field as a fine-line molding material. Said **socket** cavities 8 are formed such that they are aligned with PCB contact pads 9. Said **socket** insulator 2 is temporarily retained on said PCB 5 by a plurality of insulator retention legs 17. Said retention legs 17 may be formed of the same material used in making said **socket** insulator 2. Furthermore, in the preferred embodiment, said retention legs 17 and said **socket** insulator 2 are fabricated as one piece. Retention ribs 11 of said

retention legs 17 provide the locking means by which said **socket** insulator 2 is temporarily retained on said PCB 5. In use, said retention legs 17 are inserted into retention cavities 18 located along the perimeter of said PCB 5 and locked into place with said retention ribs 11. Said retention legs 17 may vary in length in accordance with the size of said PCB 5 and whether a plurality of circuit boards are to be stacked together, as illustrated in FIG. 1A.

US-PAT-NO: 4763041

DOCUMENT-IDENTIFIER: US 4763041 A

TITLE: Dot array fluorescent tube for writing optical information in optical printer

DATE-ISSUED: August 9, 1988

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Segawa; Hideo	Tokyo	N/A	N/A	JP

US-CL-CURRENT: 313/496, 313/497 , 340/815.73 , 347/122 , 355/67

ABSTRACT:

A dot array fluorescent tube for an optical printer writes optical information on a photoconductive element by converting an information signal representative of a desired image to optical information. A grid electrode disposed in a vacuum space defined in a housing has a slot-like opening in a portion thereof which faces an array of fluorescent elements which are formed on anodes, which are also arranged in an array in the lengthwise direction of the housing. The grid electrode is formed as a metal film on the housing through an insulating layer. A conductive light intercepting film is deposited on the housing except for a limited portion which faces the fluorescent element array, thereby regulating the direction of light which is transmitted through the housing. The fluorescent elements in the array provide a plurality of dot arrays which are controlled independently of each other. Lead terminals are connected with the anodes and led out to the outside of the housing to be connected to external drive devices by an anisotropic conductive rubber connector. The lead terminals are divided into groups each made up of a predetermined number.

11 Claims, 18 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 8

---------- KWIC ---------

Detailed Description Text - DETX (24):

As shown in FIGS. 18 and 19, connection of the terminals L.sub.i on the substrate 112 and the electrode 144 on the IC substrate 142 is accomplished by fastening retainer plates 152 and 154 to each other by screws 156 with an anisotropic conductive rubber **connector** 150. As shown in FIG. 19, the anisotropic conductive rubber **connector** 150 comprises **conductive elements** 160 arranged in a mass of insulative rubber 158 in a predetermined direction and at predetermined pitches. The terminals L.sub.i and 144 can be readily and surely interconnected merely by **compressing the connector** 150 therebetween. The **connector** 150 of the kind described, which has found applications such as to liquid **crystal** display panels, is capable of interconnecting terminals at pitches up to 200 microns. Therefore, it is sufficiently applicable even to an optical printer if, in the case of a ten terminals per millimeter arranement, for example, the lead terminals L.sub.i are distributed in the alternating manner as shown in FIG. 3, i.e., at pitches of 200 microns. The IC substrate

142 may be made of a flexible material such as polyimide in order to arrange the IC chips 140 on the back of the substrate 12 and, thereby, render the whole configuration compact. Furthermore, in accordance with this embodiment, the substrate 12 even if made of glass will be prevented from being broken in contrast to the case of thermocompression bonding and, in addition, when any of the fluorescent elements 20.sub.i or the like on the substrate 12 has failed, it is needless to replace the comparatively expensive ICs 140 and only the substrate 12 should be replaced. As described above, this particular embodiment accomplishes the fifth object of the present invention.

US-PAT-NO: 6373545

DOCUMENT-IDENTIFIER: US 6373545 B1

TITLE: Repairable TFT-LCD assembly and method for making in which a separation tape positioned between two anisotropic conductive films

DATE-ISSUED: April 16, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yang; Chin Chen	Hsin chu	N/A	N/A	TW
Shieh; Fang I.	Hsin chu	N/A	N/A	TW
Lin; Hong-Yu	Hsin chu	N/A	N/A	TW
Lee; Yu Chi	Tao-Yuan	N/A	N/A	TW
Wu; Chi Yuan	Hsinchu	N/A	N/A	TW
Fun; Su Yu	Hsinchu	N/A	N/A	TW

US-CL-CURRENT: 349/149, 349/152

ABSTRACT:

A repairable TFT-LCD assembly and a method for fabricating such assembly have been disclosed. In the repairable TFT-LCD assembly, a novel separation tape is utilized between the TFT and the LCD substrate such that when the tape is pulled in a perpendicular direction to the planar surface of the LCD substrate, the TFT can be separated from the assembly without causing damages to the LCD substrate. The separation tape is fabricated of a polymeric based insulating material with a multiplicity of apertures filled with a conductive metal. The back of the separation tape is laminated with a copper film which is patterned corresponding to the pattern of conductive pads provided on the LCD substrate. The present invention is further directed to a method for fabricating the separation tape for use in a repairable TFT-LCD assembly.

20 Claims, 21 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

---------- KWIC ---------

Brief Summary Text - BSTX (7):

In still another technique for bonding a LCD to a PCB, as shown in FIG. 1C, a chip on glass (COG) technique is used. In the COG technique, an **IC** chip 16 is **mounted** directly on a LCD 10 by utilizing solder bumps 24 and an anisotropic conductive film (ACF) 26. Detailed cross-sectional views of an ACF 26 is shown in FIGS. 2A and 2B. As shown in FIG. 2A, a TAB tape 22 which has conductive pads 28 formed on top is positioned over an ACF tape 30 which contains electrically conductive particles 32 embedded an **insulative** compound 34. Positioned under the ACF 30 is a LCD **substrate** 10 which has **conductive elements** 36 formed on top. After the TAB tape 22, the ACF 30 and the LCD **substrate** 10 are pressed together under heat, as shown in FIG. 2B, the conductive particles 32 provides electrical communication between the conductive pads 28 and the **conductive elements** 36 and therefore allowing the TAB tape 22 to electrically communicate with the LCD **substrate** I0. It should be noted that, electrical

communication between the conductive pads 28 and the **conductive elements** 26 is only established where the conductive particles 32 are compressed, i.e., only established anisotropically and selectively. The **conductive elements** 36 on the LCD **substrate** 10 is normally formed of indium-tin-oxide (ITO) thin films.

US-PAT-NO: 6362525

DOCUMENT-IDENTIFIER: US 6362525 B1

TITLE: Circuit structure including a passive element formed within a grid array substrate and method for making the same

DATE-ISSUED: March 26, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rahim; Irfan M.	Milpitas	CA	N/A	N/A

US-CL-CURRENT: 257/738, 257/528 , 257/531 , 257/668 , 257/700 , 257/701 , 257/723 , 257/728 , 257/737 , 257/777 , 257/778 , 257/E23.07 , 361/760 , 361/764 , 361/765 , 361/767 , 438/238 , 438/381

ABSTRACT:

A circuit structure combines an integrated circuit with a passive circuit element formed within a grid-array substrate. Formation of the circuit structure includes forming a passive circuit element within one or more conductive layers of a grid-array substrate such as may be used for packaging of integrated circuits. A pair of terminals of the passive circuit element is coupled to a pair of passive element contact pads within a processed surface of the integrated circuit, thereby connecting the integrated circuit to the grid-array substrate. The same grid-array substrate may be used for formation of the passive circuit element and for packaging of the integrated circuit. In some embodiments the lateral extent of the integrated circuit overlaps the lateral extent of the passive circuit element. Alternatively, the passive circuit element may be laterally displaced from the integrated circuit. A low-loss substrate may be mounted onto the grid-array substrate, and laterally displaced from the integrated circuit such that the lateral extent of the low-loss substrate overlaps that of the passive circuit element.

20 Claims, 15 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

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Brief Summary Text - BSTX (20):

In an embodiment of a method described herein, a passive circuit element is formed at least in part within a conductive layer of a grid-array **substrate**. The conductive layer is preferably formed to have a thickness greater than about 5 microns, and may be formed from copper or other conductive materials. Passive circuit elements which may be formed include inductors, capacitors, and transmission lines. Spiral inductors and some types of transmission line, for example, may be patterned within a single **conductive layer, while other elements** such as capacitors and transmission lines utilizing a ground plane may be formed using two conductive layers separated by an **insulating** layer. The passive element formation includes patterning of a conductive layer within the grid-array **substrate**. This conductive layer may be an outermost layer of the

grid-array **substrate,** such that at least a portion of the passive element is formed on a surface of the grid-array **substrate**. Alternatively, the conductive layer may be covered with an **insulating** layer after patterning, such that the passive element is formed in the interior of the grid-array **substrate**. In embodiments for which one or more of the terminals of the passive element are covered by an **insulating** layer, conductive vias may be subsequently formed to connect the buried terminals to the **IC-mounting** surface of the grid-array **substrate**.

Detailed Description Text - DETX (3):

A cross-sectional view of an embodiment of a grid-array **substrate** is shown in FIG. 1a. Grid-array **substrate** 10 includes alternating conductive and **insulating** layers. In the embodiment of FIG. 1a, conductive layer 12 forms part of an **IC-mounting** surface 14 of **substrate** 10, conductive layer 16 (denoted by dashed lines) forms an inner conductive layer within **substrate** 10, and conductive layer 18 forms part of a circuit-board **mounting** surface 20 of **substrate** 10. In the embodiment of FIG. 1a, grid-array **substrate** 10 is oriented such that surface 14 is an upper surface and surface 20 is a lower surface, but other orientations may also be used. **Insulating** layers 22 are interposed between conductive layers 12 and 16 and between layers 16 and 18. Conductive layers 12, 16 and 18 are patterned to form desired contact, interconnect, and/or passive **element structures, such that the conductive** layers may not be continuous. For example, in some areas within grid-array **substrate** 10, **insulating** layers 22 are adjacent one another, because a portion of conductive layer 16 has been locally removed. Conductive layers 12, 16 and 18 are formed of a conductive material, preferably a metal and more preferably a metal including copper. The conductive layers preferably have a thickness greater than about 5 microns, and more preferably a thickness of about 14 microns or greater. In the embodiment of FIG. 1, conductive layer 12 includes a seal ring structure 23, contact pads 24 for making contact to a **mounted IC,** and spiral inductor 26, which may be more easily visualized when discussed with respect to FIG. 1b below. Spiral inductor 26 includes inductor terminals 34. Conductive layer 18 includes board contact pads 28 for making contact to a circuit board. Connections between portions of conductive layers 12 and 18 may be made using conductive vias 30 formed within **insulating** layers 22. Lateral connections between conductive layer portions may include interconnects 32, formed within conductive layer 16.

PUB-NO: EP000414378A2

DOCUMENT-IDENTIFIER: EP 414378 A2

TITLE: An adapter for integrated circuit elements and a method using the adapter for testing assembled elements.

PUBN-DATE: February 27, 1991

INVENTOR-INFORMATION:

NAME	COUNTRY
SAITO, TAMIO C O NIPPON STEEL C	JP
YAMAMOTO, TOSHIO C O NIPPON STE	JP
OHIKATA, NAOHARU C O NIPPON STE	JP
ONO, JIRO C O NIPPON STEEL CORP	JP

ASSIGNEE-INFORMATION:

NAME	COUNTRY
NIPPON STEEL CORP	JP

APPL-NO: EP90307973

APPL-DATE: July 20, 1990

PRIORITY-DATA: JP19009989A (July 21, 1989) , JP19868589A (July 31, 1989)

INT-CL (IPC): G01R001/073, H01L021/66 , H01L023/498

EUR-CL (EPC): G01R001/073 ; G01R031/316, G01R031/3185

US-CL-CURRENT: 324/158.1

ABSTRACT:

CHG DATE=19990617 STATUS=O> A member for assembly of **IC** element having a large number of connection terminals (C1 - Cn+1) and a self-test circuit (130, 81) incorporated therein, which comprises: a **substrate** (1) made of a film of **insulating** material and having a first portion (104) for defining a position of an **IC** element (105) to be assembled and a second portion (110) surrounding the first portion; a large number of conductive leads (11) **mounted on the substrate** and spaced from each other, the leads having respective inner end portions (11a) positioned in the first portion for convenience of connection to the connection terminals of the **IC** element when the **IC** element is placed in the position defined by the first portion and respective outer end portions (11b) positioned in the second portion; and a plurality of test pads (114, 115; 71c,71c min , 71c sec) provided on the second portion and spaced from each other, wherein the number of the test pads is a limited value which is not smaller than the number of the connection terminals associated with the test circuit but irrespective of and less than the number of all the connection terminals of the **IC** element, the size of each test pad is at least larger than that of the outer end portion of the conductive lead, and any two of the test pads are spaced by a distance enough to assure reliability of test when the **IC** element is tested through the test pads. Also a method of testing the electrical connections between the connection terminals of the **IC element and the conductive** leads.

TDB-ACC-NO: NN82035075

DISCLOSURE TITLE: High Resolution Matrix Print Element Structure and Method For Manufacturing The Structure. March 1982.

PUBLICATION-DATA: IBM Technical Disclosure Bulletin, March 1982, US

VOLUME NUMBER: 24

ISSUE NUMBER: 10

PAGE NUMBER: 5075 - 5077

PUBLICATION-DATE: March 1, 1982 (19820301)

CROSS REFERENCE: 0018-8689-24-10-5075

DISCLOSURE TEXT:

3p. The reduced energy levels required by the write electrodes of certain electrolytic printers has led to a search for the best methods of implementing an integrated print head that can take full advantage of this energy reduction while still achieving relatively high print density. A matrix printer which is to have 240 printing elements per inch resolution (pel) requires a print element geometry similar to that shown in Fig. 1.

- Each of the **conductive print elements** or styli 10 must be connected by a conductive line to a driver and/or decoding logic circuitry therefore which is contained in an integrated chip. The styli must be electrically isolated from each other as well as from the conductive reference plane. This isolation is accomplished using rings of dielectric material. The thickness of the rings is limited by the voltage and current requirements for printing and their compatibility with LSI or VLSI (very large-scale integration) chip technology.

- Ruthenium dioxide (RuO(2)), either alone or dispersed in a glass matrix, has been selected as a covering surface conductor material for the styli and reference plane because of its excellent wear resistance and chemical inertness. Electrical connection from the driver chips to the styli and reference plane requires a two-level metallurgy structure to provide crossovers. Vias or thru-holes must be provided in the dielectric separating the metal layers to allow interconnection between the layers. Fig. 1 is a top view showing the print styli detail, Fig. 2 shows a cross-sectional view A-A of the print element structure, Fig. 3 illustrates a detail of the first level metallurgy in the print element area, and Fig. 4 depicts the detail of the interlevel via or thru-hole pattern.

- The first layer of metallurgy would be made using processes similar to those used in metallized ceramic (MC) technology and provide the conductor patterns for external I/O and power to the decoder/driver chips, as well as connection to the print element styli and reference plane. The standard chrome-copper-chrome MC metallurgy could be used, or the top and bottom Chrome layers could be eliminated or replaced with other suitable metals that would improve adhesion to the **substrate** or photoresist. The first level conductor lines are then covered with a photoresist 0.5 to 3.0 mils thick. Either a dry film or liquid resist could be employed. The resist is then exposed through a patterened mask and developed. It is removed wherever a connection from the first to the second metal layer is desired, i.e., print styli, chip or I/O pad sites.

Copper

is then plated up in the areas where the resist was removed until it is the same thickness as the remaining resist. Plating can be accomplished either by electroplating or electroless plating, with the latter being preffered. The remaining resist is then stripped, and the dielectric layer applied. The preferred dielectric is a recrystallizable glass with a sintering temperature of 700 to 1000 degrees C. The powered glass is made into a slurry and sprayed, screened or doctor bladed onto the **substrate**. After sintering and recrystallizing the dielectric, the surface is ground flat.

- The second metal layer is deposited identically to the first (evaporated or sputtered), but all of the **substrate** except the print element area is masked. Photoresist 0.5 to 3.0 mils thick is applied over the second metal layer, and exposed and developed so as to leave resist-free rings where isolation is desired between print styli and the reference plane. Copper is again plated up to the thickness of the resist, and the resist removed. The **IC** pads and the chip site I/O pads must be masked during the plating. RuO(2) glass paste is applied to the unmasked portions of the second metal layer and then fired to the thickness of the copper rings. The **IC** pads and the chip site I/O pads must also be masked during the RuO(2) application step. The RuO(2) surface is then ground flat, and the copper rings are etched away.

Etching is continued long enough to etch through the second metal layer, thus obtaining electrical isolation for each print element. The **IC** pads and the chip site I/O pads must also be masked during this etching operation. Finally, the rings, left open when the copper was etched away, are filled with the recrystallizable glass slurry, the dielectric sintered and the surface of the print elements ground flat.

- Using this method, the conductive wear surfaces can be made thick enough to meet the print head life requirements. In addition, and rather importantly, use of the foregoing method insures that the spacing between the print styli is essentially kept vertical, no worse than + or -20 percent, so that as the styli wear the **insulated** separation there between is kept relatively constant, within the permissible tolerance. Further, dielectric isolating the print elements and the reference plane can be made thin enough so that voltage requirements are compatible with LSI chip technology. Finally, assembly of the print head requires only **mounting of the IC** decoder/driver chips using known techniques and thereafter capping or encapsulating the chips.

I/O connections can be made via a spring clip-type connector, an elastomeric connector, or by soldering a flat cable or flex circuit to the I/O site pads.

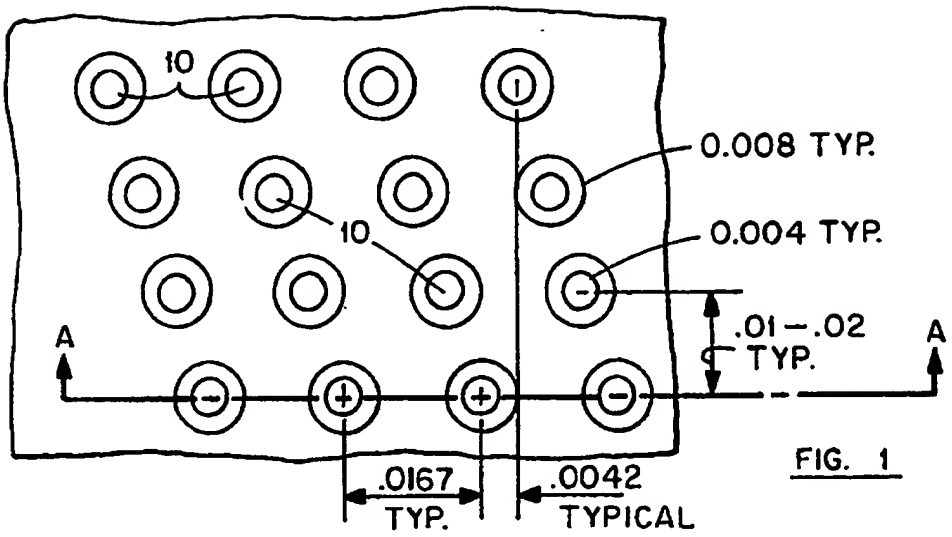

FIG. 1

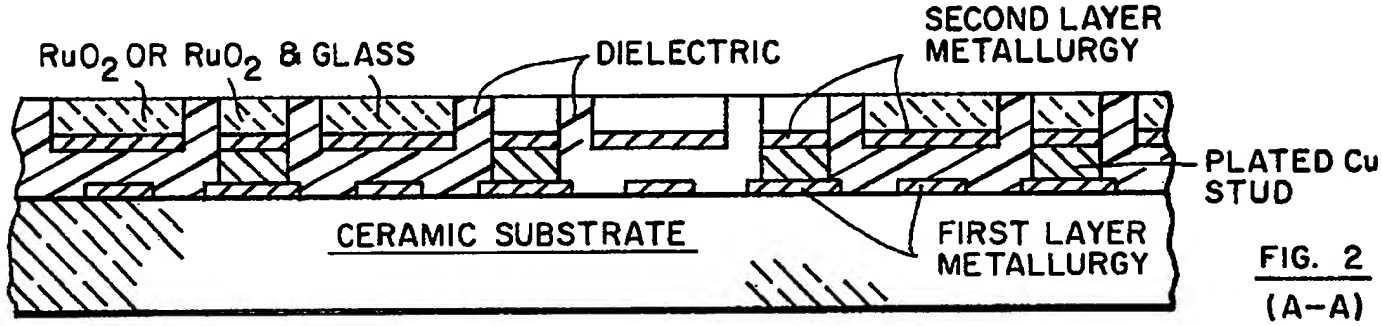

FIG. 2
(A–A)

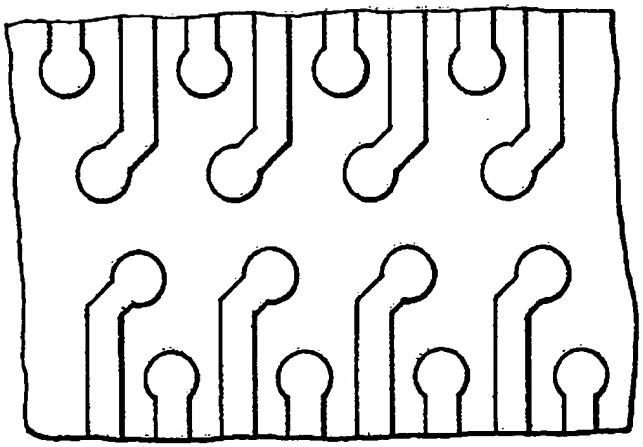

FIG. 3
FIRST LAYER METALLURY DETAIL

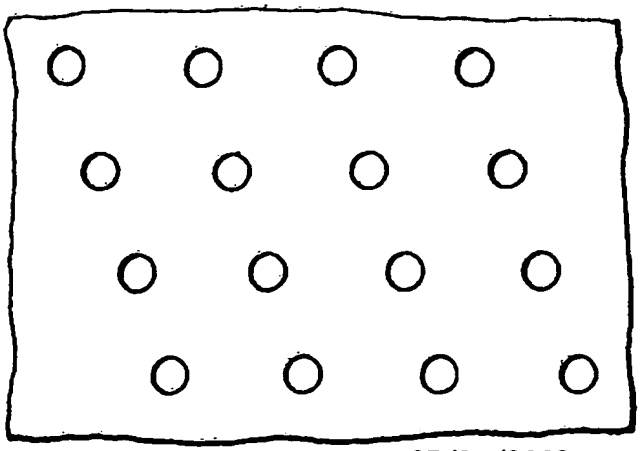

FIG. 4
SECOND PHOTO MASK DETAIL

TDB-ACC-NO: NN82035075

DISCLOSURE TITLE: High Resolution Matrix Print Element Structure and Method For Manufacturing The Structure. March 1982.

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- Ruthenium dioxide (RuO(2)), either alone or dispersed in a glass matrix, has been selected as a covering surface conductor material for the styli and reference plane because of its excellent wear resistance and chemical inertness. Electrical connection from the driver chips to the styli and reference plane requires a two-level metallurgy structure to provide crossovers. Vias or thru-holes must be provided in the dielectric separating the metal layers to allow interconnection between the layers. Fig. 1 is a top view showing the print styli detail, Fig. 2 shows a cross-sectional view A-A of the print element structure, Fig. 3 illustrates a detail of the first level metallurgy in the print element area, and Fig. 4 depicts the detail of the interlevel via or thru-hole pattern.

- The first layer of metallurgy would be made using processes similar to those used in metallized ceramic (MC) technology and provide the conductor patterns for external I/O and power to the decoder/driver chips, as well as connection to the print element styli and reference plane. The standard chrome-copper-chrome MC metallurgy could be used, or the top and bottom Chrome layers could be eliminated or replaced with other suitable metals that would improve adhesion to the substrate or photoresist. The first level conductor lines are then covered with a photoresist 0.5 to 3.0 mils thick. Either a dry film or liquid resist could be employed. The resist is then exposed through a patterened mask and developed. It is removed wherever a connection from the first to the second metal layer is desired, i.e., print styli, chip or I/O pad sites.

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- The second metal layer is deposited identically to the first (evaporated or sputtered), but all of the substrate except the print element area is masked. Photoresist 0.5 to 3.0 mils thick is applied over the second metal layer, and exposed and developed so as to leave resist-free rings where isolation is desired between print styli and the reference plane. Copper is again plated up to the thickness of the resist, and the resist removed. The IC pads and the chip site I/O pads must be masked during the plating. RuO(2) glass paste is applied to the unmasked portions of the second metal layer and then fired to the thickness of the copper rings. The IC pads and the chip site I/O pads must also be masked during the RuO(2) application step. The RuO(2) surface is then ground flat, and the copper rings are etched away.

Etching is continued long enough to etch through the second metal layer, thus obtaining electrical isolation for each print element. The IC pads and the chip site I/O pads must also be masked during this etching operation. Finally, the rings, left open when the copper was etched away, are filled with the recrystallizable glass slurry, the dielectric sintered and the surface of the print elements ground flat.

- Using this method, the conductive wear surfaces can be made thick enough to meet the print head life requirements. In addition, and rather importantly, use of the foregoing method insures that the spacing between the print styli is essentially kept vertical, no worse than + or -20 percent, so that as the styli wear the insulated separation there between is kept relatively constant, within the permissible tolerance. Further, dielectric isolating the print elements and the reference plane can be made thin enough so that voltage requirements are compatible with LSI chip technology. Finally, assembly of the print head requires only mounting of the IC decoder/driver chips using known techniques and thereafter capping or encapsulating the chips.

I/O connections can be made via a spring clip-type connector, an elastomeric connector, or by soldering a flat cable or flex circuit to the I/O site pads.

DERWENT-ACC-NO: 2000-263132

DERWENT-WEEK: 200023

TITLE: **Mounting** mechanism of **IC** chip, has electrically **conductive element** to connect wiring pattern formed on **insulated substrate** and chip electrode where copper board is attached to under surface of **substrate**

PATENT-ASSIGNEE: MITSUMI ELECTRIC CO LTD[DENA]

PRIORITY-DATA: 1998JP-0236213 (August 24, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2000068425 A	March 3, 2000	N/A	004	H01L 023/36

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP2000068425A	N/A	1998JP-0236213	August 24, 1998

INT-CL (IPC): H01L023/36

ABSTRACTED-PUB-NO: JP2000068425A

BASIC-ABSTRACT:

NOVELTY - A wiring pattern (3) is formed on a surface of an insulated substrate (2) having a hole for positioning chip component (105). A copper board (1) is attached to another surface of the insulated substrate, contacting the chip component. An electrically conductive element (5) is used to connect the wiring pattern and electrode of chip component.

USE - Used for mounting chip components like IC chip.

ADVANTAGE - Heat generated by chip is efficiently released as chip is directly mounted on copper board. Heat releasing property is enhanced as heat is transmitted to wiring pattern in shorter time as length of bonding wire is reduced. Space is saved as chip is placed inside the insulated substrate and doesn't project out.

DESCRIPTION OF DRAWING(S) - The figure shows perspective and sectional diagram of mounting mechanism.

Copper board 1

Insulated substrate 2

Wiring pattern 3

Electrically conductive element 5

Chip component 105

CHOSEN-DRAWING: Dwg.1/3

TITLE-TERMS: MOUNT MECHANISM IC CHIP ELECTRIC CONDUCTING ELEMENT CONNECT WIRE PATTERN FORMING INSULATE SUBSTRATE CHIP ELECTRODE COPPER BOARD ATTACH SURFACE SUBSTRATE

DERWENT-CLASS: U11

EPI-CODES: U11-D02B1;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N2000-196629

DERWENT-ACC-NO: 2000-263132

DERWENT-WEEK: 200023

TITLE: Mounting mechanism of IC chip, has electrically conductive element to connect wiring pattern formed on insulated substrate and chip electrode where copper board is attached to under surface of substrate

PATENT-ASSIGNEE: MITSUMI ELECTRIC CO LTD[DENA]

PRIORITY-DATA: 1998JP-0236213 (August 24, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2000068425 A	March 3, 2000	N/A	004	H01L 023/36

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP2000068425A	N/A	1998JP-0236213	August 24, 1998

INT-CL (IPC): H01L023/36

ABSTRACTED-PUB-NO: JP2000068425A

BASIC-ABSTRACT:

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DERWENT-CLASS: U11

EPI-CODES: U11-D02B1;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N2000-196629

US-PAT-NO: 6336269

DOCUMENT-IDENTIFIER: US 6336269 B1

TITLE: Method of fabricating an interconnection element

DATE-ISSUED: January 8, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Eldridge; Benjamin N.	Hopewell Junction	NY	12533	N/A
Grube; Gary W.	Monroe	NY	10950	N/A
Khandros; Igor Y.	Peekskill	NY	10566	N/A
Mathieu; Gaetan L.	Carmel	NY	10512	N/A

US-CL-CURRENT: 29/885, 228/180.5 , 228/199 , 257/E21.503 , 257/E21.509 , 257/E21.511 , 257/E21.512 , 257/E21.519 , 257/E21.525 , 257/E23.021 , 257/E23.024 , 257/E23.068 , **257/E23.078** , 257/E25.011 , 257/E25.029 , 29/825 , 29/830 , 29/840 , 29/843

ABSTRACT:

Contact structures formed on an electronic component are useful for connecting the component to other electronic components. A contact tip structure can be formed on a sacrificial substrate, then combined with an interconnection element. A preferred contact structure includes some topography, generally in the form of certain raised features. These are formed by embossing depressed features into the sacrificial substrate upon which the contact tip structure is constructed. The contact tip structure can be optimized for making contact with another electrical component.

23 Claims, 177 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 60

---------- KWIC ---------

Brief Summary Text - BSTX (22):

One recent effort directed to making resilient connections is described in an article entitled ELASTOMERIC CONNECTOR FOR MCM AND TEST APPLICATIONS, ICEMM Proceedings, 1993, pages 341-346, which describes an "Elasticon" (tm) connector. The Elasticon connector uses solid gold or gold alloy wires for the **conductive elements,** embedded in an elastomer material (e.g., liquid elastomer resin injected into a mold cavity), and is generally targeted at the interconnection requirements for land grid array (LGA) packages for multichip (MCM) and single (SCM) chip modules. The size, shape and spacing of the wires, along with the elastomer material properties, can be tailored to specific application requirements which include MCM and SCM packaging, board-to-board and cable-to-board interconnections, as well as high density PCB and **IC** chip testing applications. The solid gold wires and the silicone elastomer material are impervious to corrosion. FIG. 1 of the article illustrates a basic embodiment of the Elasticon connector, wherein a plurality of wires are ball-bonded to a rigid **substrate** and extend straight at an angle (e.g., 45-85.degree.) from the surface of the **substrate**. Attachment of the proximal

ends of the wires to the **substrate** is by an angled flying lead wire bonding process using compressive force and ultrasonic energy applied through the capillary tip and thermal energy applied through the heated stage on the wirebonder. The capillary and **substrate** are positioned to allow a shear blade mechanism to sever the wire at the desired height and angle from the **substrate** surface. Electronic flame-off (EFO) is used to melt the wire extending from the capillary tip to start the next ball bond (of the proximal end of the next wire to be bonded to the **substrate**). After mounting all of the wires to the **substrate,** a ball-shaped contact is formed at the far (distal) end of each wire by a process of laser ball forming, and the plurality of wires are embedded in an elastomer material. The ball-shaped (enlarged) distal ends help prevent the wires from vibrating loose and causing shorts between contacts. As noted in the article, the angled orientation of the conductors is necessary to minimize plastic deformation of the wires as an Elasticon connector is compressed between two parallel surfaces. The angled orientation also provides a "wiping" contact surface which, when the connector is compressed, will cause the wires to rotate and slide against the mating contact surfaces. The article discusses the use of gold/palladium alloys and platinum for the wires. FIG. 3 of the article describes clustering wires in groups of one to four wires per contact, in conjunction with forming grooves in the elastomer between each group of wires. The various embodiments of the Elasticon connector described in the article require a **substrate** of ceramic, metal, silicon or epoxy-glass laminate material, and interposer embodiments require an etchable **substrate** material such as copper with a thin layer of gold on the top surface. FIG. 8 of the article describes integrated probe contacts and aptly notes that the ability to test for known good dies has been one of the stumbling blocks for MCM packaging. As shown therein, a probe matrix uses 2 mil (0.002 inch) diameter gold wires in an array. The probes can permanently be attached to the test module, or fabricated as an interposer structure. U.S. Pat. No. 5,386,344 (Beaman, et al.; January 1995; USCL 361/785), entitled FLEX CIRCUIT CARD ELASTOMERIC CABLE CONNECTOR ASSEMBLY, discloses a related "Elastipac" (tm) elastomeric cable connector.

Current US Cross Reference Classification - CCXR (12):
257/E23.078

PGPUB-DOCUMENT-NUMBER: 20010020545

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010020545 A1

TITLE: Electrical contact structures formed by configuring a flexible wire to have a springable shape and overcoating the wire with at least one layer of a resilient conductive material, methods of mounting the contact structures to electronic components, and applications for employing the contact structures

PUBLICATION-DATE: September 13, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
RULE-47			
Eldridge, Benjamin N.	Danville	CA	US
Grube, Gary W.	Pleasanton	CA	US
Khandros, Igor Y.	Orinda	CA	US
Mathieu, Gaetan L.	Livermore	CA	US

US-CL-CURRENT: 174/260, 257/618 , 257/E21.503 , 257/E21.508 , 257/E21.509 , 257/E21.511 , 257/E21.512 , 257/E21.519 , 257/E21.525 , 257/E23.021 , 257/E23.024 , 257/E23.068 , **257/E23.078** , 257/E25.011 , 257/E25.029 , 361/718 , 361/736

ABSTRACT:

Contact structures exhibiting resilience or compliance for a variety of electronic components are formed by bonding a free end of a wire to a substrate, configuring the wire into a wire stem having a springable shape, severing the wire stem, and overcoating the wire stem with at least one layer of a material chosen primarily for its structural (resiliency, compliance) characteristics.

---------- KWIC ---------

Current US Classification, US Secondary Class/Subclass - CCSR (12):
257/E23.078

Summary of Invention Paragraph - BSTX (22):

[0021] One recent effort directed to making resilient **connections** is described in an article entitled ELASTOMERIC **CONNECTOR** FOR MCM AND TEST APPLICATIONS, ICEMM Proceedings, 1993, pages 341-346, which describes an "Elasticon" (tm) **connector**. The Elasticon **connector** uses solid gold or gold alloy wires for the conductive elements, embedded in an elastomer material (e.g., liquid elastomer resin injected into a mold cavity), and is generally targeted at the interconnection requirements for land grid array (LGA) packages for multichip (MCM) and single (SCM) chip modules. The size, shape and spacing of the wires, along with the elastomer material properties, can be tailored to specific application requirements which include MCM and SCM packaging, board-to-board and cable-to-board interconnections, as well as high density PCB and IC chip testing applications. The solid gold wires and the silicone elastomer material are impervious to corrosion. FIG. 1 of the article illustrates a basic embodiment of the Elasticon **connector,** wherein a plurality of wires are ball-bonded to a rigid substrate and extend straight at an angle

(e.g., 45-85.degree.) from the surface of the substrate. Attachment of the proximal ends of the wires to the substrate is by an angled flying lead wire bonding process using **compressive** force and ultrasonic energy applied through the capillary tip and thermal energy applied through the heated stage on the wirebonder. The capillary and substrate are positioned to allow a shear blade mechanism to sever the wire at the desired height and angle from the substrate surface. Electronic flame-off (EFO) is used to melt the wire extending from the capillary tip to start the next ball bond (of the proximal end of the next wire to be bonded to the substrate). After mounting all of the wires to the substrate, a ball-shaped contact is formed at the far (distal) end of each wire by a process of laser ball forming, and the plurality of wires are embedded in an elastomer material. The ball-shaped (enlarged) distal ends help prevent the wires from vibrating loose and causing shorts between contacts. As noted in the article, the angled orientation of the conductors is necessary to minimize plastic deformation of the wires as an Elasticon **connector is compressed** between two parallel surfaces. The angled orientation also provides a "wiping" contact surface which, when the **connector is compressed,** will cause the wires to rotate and slide against the mating contact surfaces. The article discusses the use of gold/palladium alloys and platinum for the wires. FIG. 3 of the article describes clustering wires in groups of one to four wires per contact, in conjunction with forming grooves in the elastomer between each group of wires. The various embodiments of the Elasticon **connector** described in the article require a substrate of ceramic, metal, silicon or epoxy-glass laminate material, and interposer embodiments require an etchable substrate material such as copper with a thin layer of gold on the top surface. FIG. 8 of the article describes integrated probe contacts and aptly notes that the ability to test for known good dies has been one of the stumbling blocks for MCM packaging. As shown therein, a probe matrix uses 2 mil (0.002 inch) diameter gold wires in an array. The probes can permanently be attached to the test module, or fabricated as an interposer structure. U.S. Pat. No. 5,386,344 (Beaman, et al.; 1/95; USCL 361/785), entitled FLEX CIRCUIT CARD ELASTOMERIC CABLE **CONNECTOR** ASSEMBLY, discloses a related "Elastipac" (tm) elastomeric cable **connector**.

Summary of Invention Paragraph - BSTX (31):

[0030] U.S. Pat. No. 5,366,380 (Reymond; 11/94; USCL 439/66), entitled SPRING BIASED TAPERED CONTACT ELEMENTS FOR ELECTRICAL **CONNECTORS** AND INTEGRATED CIRCUIT PACKAGES, discloses a contact element for an electrical **connector** of for an integrated circuit package (**ICP**), which is particularly useful for surface mount applications. The contact element has a base portion, a spring portion having at least partially helical spring elements, and a tapered contact portion which mates in a biased manner with a conductive rim of a hole, and can be fabricated from a flat sheet with punching, rolling, and/or forming operations, thin-walled drawn parts, or modular parts. The contact elements are maintained in a **compressed** state by a hold-down mechanism. The contact elements can be associated with insulating housings and/or spacers which provide functions such as alignment, **compression** limitation, contact support, and installation fixturing.

US-PAT-NO: 5366380

DOCUMENT-IDENTIFIER: US 5366380 A

TITLE: Spring biased tapered contact elements for electrical connectors and integrated circuit packages

DATE-ISSUED: November 22, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reymond; Welles K.	Waterbury	CT	N/A	N/A

US-CL-CURRENT: 439/66, **257/E23.078** , 361/773 , 439/700

ABSTRACT:

A contact element for an electrical connector or an integrated circuit which is used with a hold-down mechanism has a base portion, a spring portion having at least partially helical spring elements, and a tapered contact portion which mates in a biased manner with the conductive rim of a hole. The contact element is particularly useful for surface mount applications. The spring portion is preferably arranged with a partially helical spring configuration so that compression of the spring also effects a torsional rotation of the contact portion. The contact element can be fabricated from: a flat sheet with punching, rolling, and/or forming operations, thin walled drawn parts, or modular parts. Additionally, spring sections may be arranged in tandem, in either a co-rotational or counter-rotational manner to provide additional degrees of design freedom with respect to compression range, axial spring rate, and rotational rate. Contact elements can be associated with insulating housings and/or spacers which provide functions such as alignment, compression limitation, contact support, and installation fixturing. In a preferred embodiment the contact portion has a non-linear taper which permits the normal mating force to be well defined regardless of the diameter of the conductive rim of the hole.

46 Claims, 20 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 8

---------- KWIC ---------

Brief Summary Text - BSTX (34):

Preferred aspects of the invention include: forming the tapered contact portion with a circular, parabolic or other non-linear taper; forming the spring portion from flat strips which are each curved to each form partial helical elements; and constructing the contact element by stamping or etching a thin sheet of conductive material and then rolling the material to form a cylinder with a tapered contact portion. Where the contact element is formed by stamping or etching, the "walls" of the contact element include the flat helical spring elements which **compresse** radially inwardly and causes the contact portion to rotate when the contact element is pressed against the rim of a hole. In accord with different embodiments of the invention, many such contact elements are arranged in a pattern as the contacts of an **ICP** or as the contacts of an electrical **connector** coupled to a PCB to mate with conductive

rims of holes on another PCB or similar device. The contact elements of the **ICP** or PCB, once pressed against the conductive rims are held in biased contact by any of several fastening means described in the above-mentioned parents of this application.

Detailed Description Text - DETX (4):

As seen in FIGS. 3a and 3b, it will further be appreciated that when the **ICP** 12 is pressed against the PCB 24, the spring portion 20 of contact element 10 biases the contact portion 16 against the rim 22 of hole 26 in PCB 24 assuring a good electrical **connection** between the contact portion 16 and the rim 22. According to a preferred embodiment of the invention, as the spring portion 20 of the contact element is biased (by applying a downward force), a torsional rotation (shown by arrow 28 in FIG. 3b) is effected at the contact portion 16. This rotation of the contact portion 16 causes the contact portion to rotationally wipe the rim 22 as the contact portion extends into the hole and axially wipes the rim, thus ensuring a good electrical coupling. It should be understood by those skilled in the art that any type of spring which effects a rotation during **compression** can be, used as the spring portion of the contact element to effect the torsional rotation of the contact portion. However, according to a first preferred embodiment of the contact element, the contact portion 16, spring 20 and base 18 are preferably manufactured as an integral piece from a sheet of conductive material as discussed hereinafter with reference to FIGS. 3c and 3d. With the spring elements being formed from flat stock as opposed to round, the spring elements do not act like a classical simple coil spring. Also, by providing a plurality of flat spring elements, parallel electrical paths are provided, thereby reducing inductance as opposed to a single coil spring. Further, by designing the spring elements as desired (e.g., width, thickness, length, twist, etc., the parameters governing contact forces can be controlled. Indeed, depending on the contact environment, more or less wipe may be desired. For example, for nobel metal systems where lots of mating cycles may be required, less wipe may be desirable, whereas in a non-nobel metal environment such as tin or tin-lead, where only a few mating cycles are expected, a large wipe may be desired and tolerated.

Current US Cross Reference Classification - CCXR (1):

257/E23.078

US-PAT-NO: 6078500

DOCUMENT-IDENTIFIER: US 6078500 A

TITLE: Pluggable chip scale package

DATE-ISSUED: June 20, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Beaman; Brian Samuel	Apex	NC	N/A	N/A
Fogel; Keith Edward	Mohegan Lake	NY	N/A	N/A
Lauro; Paul Alfred	Nanuet	NY	N/A	N/A
Shih; Da-Yuan	Poughkeepsie	NY	N/A	N/A

US-CL-CURRENT: 361/704, 165/185 , 165/80.3 , 174/16.3 , 257/706 , 257/709 , 257/723 , **257/E23.078** , 257/E23.124 , 29/830 , 29/848 , 29/850 , 361/707 , 361/710 , 361/764

ABSTRACT:

A structure for packaging an electronic device. The package has: an electronic device having a first surface and an opposite second surface, the first surface having a plurality of first electrical contact locations; a substrate having a surface having a plurality of substrate electrical contact locations; a flexible interposer comprising a flexible material and a plurality of elongated electrical conductors disposed therein and extending from the first side to the second side, each of the elongated electrical conductors has a first end at the first side of the flexible interposer and a second end at the second side of the flexible interposer; the flexible interposer is disposed between the electronic device and the substrate; means for pushing the electronic device towards the substrate so that the flexible interposer is disposed between the first surface of the electronic device and the surface of the substrate so that the first ends of the elongated electrical conductors of the flexible interposer contact the first electrical contact locations at the first surface of the electronic device and so that the second ends of the elongated electrical conductors of the flexible interposer contact the substrate electrical contact locations; and, means for aligning the electronic device to the substrate so that the first and the second ends of the elongated electrical conductors of the flexible interposer align to the first electrical contact pads on the electronic device and to the substrate contact locations, respectively.

6 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 9

---------- KWIC ---------

Brief Summary Text - BSTX (16):

U.S. application Ser. No. 08/754,869 filed on Nov. 11, 1996, the teaching of which is incorporated herein by reference describes a high density test probe for integrated circuit devices. The **IC** wafer probe structure is similar to the compliant interface used for the pluggable chip scale package. The probe structure described in this docket uses short metal wires that are bonded

on one end to the fan out wiring on a rigid **substrate**. The wires are encased in a compliant polymer material to allow the probes to **compress** under pressure against the integrated circuit device. The wire probes must be sufficiently long and formed at an angle to prevent permanent deformation during **compression** against the integrated circuit device. Although the compliant interface uses a similar integrated wire conductor, ball shaped contact, and elastomeric material surrounding the wires, the **IC** packaging requirements includes additional features that are unique to the pluggable chip scale package.

Current US Cross Reference Classification - CCXR (7):
257/E23.078

US-PAT-NO: 5237203

DOCUMENT-IDENTIFIER: US 5237203 A

TITLE: Multilayer overlay interconnect for high-density packaging of circuit elements

DATE-ISSUED: August 17, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Massaron; Laurence I.	Santa Monica	CA	N/A	N/A

US-CL-CURRENT: 257/688, 257/690 , 257/719 , 257/727 , 257/759 , 257/773 , 257/785 , 257/E23.065 , **257/E23.078** , 257/E25.012

ABSTRACT:

A multilayer overlay interconnect for packaging various circuit elements such as integrated-circuit (**IC**) chips in high-density configurations. The overlay interconnect allows multiple **IC** chips to be removably mounted and electrically interconnected within a chip package with minimized interconnection lengths between the **IC** chips, for improved high speed operation of the chips. In addition, the back side of the chips remain accessible for making direct contact with a heat sink and/or a **substrate** interconnect which provides for good heat dissipation and/or additional electrical contact areas. The multilayer overlay interconnect is either flexible or both flexible and **compressible**. The overlay interconnect includes a plurality of thin polymer layers, a plurality of inner contact areas on an outermost layer for making electrical contact with contact areas on the **IC** chips, a plurality of outer contact areas on the outermost layer for making electrical contact with contact areas on leads extending into the chip package, and electrically-conductive traces on one or more of the layers, with interconnecting vias, for interconnecting the inner and outer contact areas. The overlay interconnect further includes cut-out regions to accommodate for substantial variations in circuit element thicknesses or circuit elements which require a medium of air to operate properly.

32 Claims, 10 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

---------- KWIC ---------

Abstract Text - ABTX (1):

A multilayer overlay interconnect for packaging various circuit elements such as integrated-circuit (**IC**) chips in high-density configurations. The overlay interconnect allows multiple **IC** chips to be removably mounted and electrically interconnected within a chip package with minimized interconnection lengths between the **IC** chips, for improved high speed operation of the chips. In addition, the back side of the chips remain accessible for making direct contact with a heat sink and/or a **substrate** interconnect which provides for good heat dissipation and/or additional electrical contact areas. The multilayer overlay interconnect is either flexible or both flexible and

compressible. The overlay interconnect includes a plurality of thin polymer layers, a plurality of inner contact areas on an outermost layer for making electrical contact with contact areas on the **IC** chips, a plurality of outer contact areas on the outermost layer for making electrical contact with contact areas on leads extending into the chip package, and electrically-conductive traces on one or more of the layers, with interconnecting vias, for interconnecting the inner and outer contact areas. The overlay interconnect further includes cut-out regions to accommodate for substantial variations in circuit element thicknesses or circuit elements which require a medium of air to operate properly.

Brief Summary Text - BSTX (10):

The present invention resides in a multilayer overlay interconnect which is either flexible or both flexible and **compressible** for packaging various circuit elements such as integrated-circuit (**IC**) chips in high-density configurations. The overlay interconnect allows multiple **IC** chips to be removably mounted and electrically interconnected within a chip package with minimized interconnection lengths between the **IC** chips, for improved high speed operation of the chips. The overlay interconnect further allows high-density packaging of circuit elements with substantial variations in thickness or which require a medium of air to operate properly, by providing cut-out regions in the overlay interconnect. In addition, the back side of the circuit elements remain accessible for making direct contact with a heat sink and/or a **substrate** interconnect which provides for good heat dissipation and/or additional electrical contact areas.

Brief Summary Text - BSTX (11):

The multilayer overlay interconnect includes a plurality of thin polymer layers which are either flexible or both flexible and **compressible,** a plurality of inner contact areas on an outermost layer for making electrical contact with contact areas on the **IC** chips, a plurality of outer contact areas on the outermost layer for making electrical contact with contact areas on leads extending into the chip package, and electrically-conductive traces on one or more of the layers, with interconnecting vias, for interconnecting the inner and outer contact layers. The **IC** chips are closely spaced and mounted on a heat sink and/or a **substrate** interconnect which provides for good heat dissipation and/or additional electrical contact areas.

Detailed Description Text - DETX (2):

As shown in the drawings for purposes of illustration, the present invention is embodied in a multilayer overlay interconnect which is either flexible or both flexible and **compressible**. By way of a non-limiting example, the multilayer overlay interconnect can be employed to package multiple integrated-circuit (**IC**) chips in high-density configurations. However, one skilled in the art would find it apparent that the overlay interconnect can be employed to package various other circuit elements such as chip resistors, chip capacitors, optical waveguides, diodes, etc., or any combination thereof. The overlay interconnect allows multiple **IC** chips to be removably mounted and electrically interconnected within a chip package with minimized interconnection lengths between the **IC** chips, for improved high speed operation of the chips. The overlay interconnect further allows high-density packaging of circuit elements with substantial variations in thicknesses or which require a medium of air to operate properly, by providing cut-out regions in the overlay interconnect. In addition, the back side of the circuit elements remain accessible for making direct contact with a heat sink and/or a **substrate** interconnect which provides for good heat dissipation and/or additional electrical contact areas.

Current US Cross Reference Classification - CCXR (8):

257/B23.078

US-PAT-NO: 4813129

DOCUMENT-IDENTIFIER: US 4813129 A

TITLE: Interconnect structure for PC boards and integrated circuits

DATE-ISSUED: March 21, 1989

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Karnezos; Marcos	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 29/832, 257/E23.021 , **257/E23.078** , 361/774 , 439/74

ABSTRACT:

An interconnect structure for electrically coupling conductive paths on two adjacent, rigid **substrates,** such as PC boards or **IC** chips. The interconnect structure includes a number of buttons formed on a first **substrate,** and a number of contacts formed on a second **substrate**. The buttons are elastically deformable, and include a resilient core made from an organic material such as polyimide, and a metallic coating formed over the core. The two **substrates are compressed** between mounting plates such that the buttons are pressed against the contracts to make electrical contact.

3 Claims, 7 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

---------- KWIC ---------

Abstract Text - ABTX (1):
An interconnect structure for electrically coupling conductive paths on two adjacent, rigid **substrates,** such as PC boards or **IC** chips. The interconnect structure includes a number of buttons formed on a first **substrate,** and a number of contacts formed on a second **substrate**. The buttons are elastically deformable, and include a resilient core made from an organic material such as polyimide, and a metallic coating formed over the core. The two **substrates are compressed** between mounting plates such that the buttons are pressed against the contracts to make electrical contact.

Current US Cross Reference Classification - CCXR (2):
257/E23.078

US-PAT-NO: 5329423

DOCUMENT-IDENTIFIER: US 5329423 A

TITLE: Compressive bump-and-socket interconnection scheme for integrated circuits

DATE-ISSUED: July 12, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Scholz; Kenneth D.	Palo Alto	CA	94306	N/A

US-CL-CURRENT: 361/760, 174/263 , 174/52.4 , 257/695 , 257/738 , 257/E21.511 , 257/E23.021 , **257/E23.078** , 361/762 , 361/767 , 361/792 , 361/808

ABSTRACT:

A electrically interconnected assembly includes an electronic component, such as an integrated circuit chip, having a first pattern of contact sites and includes a substrate having a second pattern of contact sites corresponding to the first pattern. The electronic component is demountably connected to the substrate by a bump-and-socket arrangement at each pair of contact sites. One of the contact sites has a raised bump that is received within a depressed area of the other contact site. The raised bumps are pressed into the depressed areas, forming a ring of contact to electrically and mechanically connect the electronic component to the substrate. Preferably, the depressed areas are formed in a compliant material that allows some deformation but not so much as to allow the raised bumps to bottom out against the depressed areas. The assembly may be used in forming multi-chip modules having demountable integrated circuit chips.

17 Claims, 7 Drawing figures

Exemplary Claim Number: 9

Number of Drawing Sheets: 6

---------- KWIC ---------

Brief Summary Text - BSTX (5):

An important concern in the fabrication of a multi-chip module is the method of electrically connecting the **integrated circuit** chips to the module. This concern is equally important in connecting chips to other **substrates** as well. Three well known techniques are commonly referred to as wire bonding, tape automated bonding and surface mounting. The wire bonding method is one in which miniature wires are connected at first ends to input/output pads of an **integrated circuit** chip. The opposite ends of the bond wires are welded to a **substrate,** such as a multi-chip module. Wire bonding can be performed with gold wire by thermal **compression,** ultrasonic or thermal sonic techniques, or with aluminum wire by the ultrasonic technique.

Detailed Description Text - DETX (19):

Referring now to FIG. 4, the firm wedging fit described above is achieved by **compressing integrated circuit** chip 46 utilizing a heat spreader or other cap

mechanism, not shown. The contact bumps 58 and 60 press against the socket metallization layer 66 and 68 to form a ring of contact. The compliant layer 70 is deformed slightly, as is the socket metallization layer. However, as the **integrated circuit** chip is removed, the compliant layer returns to its original shape. Thus, the assembly of FIG. 4 is a demountable assembly that permits a defective chip to be removed from the **substrate** 52.

Current US Cross Reference Classification - CCXR (7):
257/E23.078

US-PAT-NO: 5237203

DOCUMENT-IDENTIFIER: US 5237203 A

TITLE: Multilayer overlay interconnect for high-density packaging of circuit elements

DATE-ISSUED: August 17, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Massaron; Laurence I.	Santa Monica	CA	N/A	N/A

US-CL-CURRENT: 257/688, 257/690 , 257/719 , 257/727 , 257/759 , 257/773 , 257/785 , 257/E23.065 , **257/E23.078** , 257/E25.012

ABSTRACT:

A multilayer overlay interconnect for packaging various circuit elements such as **integrated-circuit (IC)** chips in high-density configurations. The overlay interconnect allows multiple **IC** chips to be removably mounted and electrically interconnected within a chip package with minimized interconnection lengths between the **IC** chips, for improved high speed operation of the chips. In addition, the back side of the chips remain accessible for making direct contact with a heat sink and/or a **substrate** interconnect which provides for good heat dissipation and/or additional electrical contact areas. The multilayer overlay interconnect is either flexible or both flexible and **compressible**. The overlay interconnect includes a plurality of thin polymer layers, a plurality of inner contact areas on an outermost layer for making electrical contact with contact areas on the **IC** chips, a plurality of outer contact areas on the outermost layer for making electrical contact with contact areas on leads extending into the chip package, and electrically-conductive traces on one or more of the layers, with interconnecting vias, for interconnecting the inner and outer contact areas. The overlay interconnect further includes cut-out regions to accommodate for substantial variations in circuit element thicknesses or circuit elements which require a medium of air to operate properly.

32 Claims, 10 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

---------- KWIC ---------

Abstract Text - ABTX (1):

A multilayer overlay interconnect for packaging various circuit elements such as **integrated-circuit (IC)** chips in high-density configurations. The overlay interconnect allows multiple **IC** chips to be removably mounted and electrically interconnected within a chip package with minimized interconnection lengths between the **IC** chips, for improved high speed operation of the chips. In addition, the back side of the chips remain accessible for making direct contact with a heat sink and/or a **substrate** interconnect which provides for good heat dissipation and/or additional electrical contact areas. The multilayer overlay interconnect is either flexible or both flexible and

compressible. The overlay interconnect includes a plurality of thin polymer layers, a plurality of inner contact areas on an outermost layer for making electrical contact with contact areas on the **IC** chips, a plurality of outer contact areas on the outermost layer for making electrical contact with contact areas on leads extending into the chip package, and electrically-conductive traces on one or more of the layers, with interconnecting vias, for interconnecting the inner and outer contact areas. The overlay interconnect further includes cut-out regions to accommodate for substantial variations in circuit element thicknesses or circuit elements which require a medium of air to operate properly.

Brief Summary Text - BSTX (10):

The present invention resides in a multilayer overlay interconnect which is either flexible or both flexible and **compressible** for packaging various circuit elements such as **integrated-circuit (IC)** chips in high-density configurations. The overlay interconnect allows multiple **IC** chips to be removably mounted and electrically interconnected within a chip package with minimized interconnection lengths between the **IC** chips, for improved high speed operation of the chips. The overlay interconnect further allows high-density packaging of circuit elements with substantial variations in thickness or which require a medium of air to operate properly, by providing cut-out regions in the overlay interconnect. In addition, the back side of the circuit elements remain accessible for making direct contact with a heat sink and/or a **substrate** interconnect which provides for good heat dissipation and/or additional electrical contact areas.

Brief Summary Text - BSTX (11):

The multilayer overlay interconnect includes a plurality of thin polymer layers which are either flexible or both flexible and **compressible,** a plurality of inner contact areas on an outermost layer for making electrical contact with contact areas on the **IC** chips, a plurality of outer contact areas on the outermost layer for making electrical contact with contact areas on leads extending into the chip package, and electrically-conductive traces on one or more of the layers, with interconnecting vias, for interconnecting the inner and outer contact layers. The **IC** chips are closely spaced and mounted on a heat sink and/or a **substrate** interconnect which provides for good heat dissipation and/or additional electrical contact areas.

Detailed Description Text - DETX (2):

As shown in the drawings for purposes of illustration, the present invention is embodied in a multilayer overlay interconnect which is either flexible or both flexible and **compressible**. By way of a non-limiting example, the multilayer overlay interconnect can be employed to package multiple **integrated-circuit (IC)** chips in high-density configurations. However, one skilled in the art would find it apparent that the overlay interconnect can be employed to package various other circuit elements such as chip resistors, chip capacitors, optical waveguides, diodes, etc., or any combination thereof. The overlay interconnect allows multiple **IC** chips to be removably mounted and electrically interconnected within a chip package with minimized interconnection lengths between the **IC** chips, for improved high speed operation of the chips. The overlay interconnect further allows high-density packaging of circuit elements with substantial variations in thicknesses or which require a medium of air to operate properly, by providing cut-out regions in the overlay interconnect. In addition, the back side of the circuit elements remain accessible for making direct contact with a heat sink and/or a **substrate** interconnect which provides for good heat dissipation and/or additional electrical contact areas.

Current US Cross Reference Classification - CCXR (8):

US-PAT-NO: 4924353

DOCUMENT-IDENTIFIER: US 4924353 A

TITLE: Connector system for coupling to an integrated circuit chip

DATE-ISSUED: May 8, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Patraw; Nils E.	Redondo Beach	CA	N/A	N/A

US-CL-CURRENT: 361/783, 257/E21.511 , **257/E23.078** , 361/764 , 361/776

ABSTRACT:

A connector system for selectively coupling in a desired manner the input/output terminals of an **integrated circuit** chip to the input/output terminals of one or more other **integrated circuit** chips or to a circuit interface pin. The system includes, for each of the chips, an insulating mesa member mechanically attached to a surface of the chip. Each of the mesa members has a surface having a plurality of conductive pads disposed thereon, each of the pads being conductively coupled to the input/output terminals of the associated chip. A **substrate** having a recess made therein is provided with a plurality of conductive pathways. The recess defines a region of the underlying **substrate,** the region being provided with resilient **compressible** conductive pedestals, the pedestals being conductively coupled to the pathways within the region. Each of the pedestals is further disposed in registration with the conductive pads upon a mesa member such that when the mesa is inserted within the recess, the pedestals conductively couple the input/output terminals of the associated chip to the underlying pathways. A **compression** spring is also provided for urging the chip towards the **substrate,** thereby coupling the conductive pads to the pathways through the resilient **compressible** pedestals.

7 Claims, 8 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 2

---------- KWIC ---------

Abstract Text - ABTX (1):

A connector system for selectively coupling in a desired manner the input/output terminals of an **integrated circuit** chip to the input/output terminals of one or more other **integrated circuit** chips or to a circuit interface pin. The system includes, for each of the chips, an insulating mesa member mechanically attached to a surface of the chip. Each of the mesa members has a surface having a plurality of conductive pads disposed thereon, each of the pads being conductively coupled to the input/output terminals of the associated chip. A **substrate** having a recess made therein is provided with a plurality of conductive pathways. The recess defines a region of the underlying **substrate,** the region being provided with resilient **compressible** conductive pedestals, the pedestals being conductively coupled to the pathways within the region. Each of the pedestals is further disposed in registration

with the conductive pads upon a mesa member such that when the mesa is inserted within the recess, the pedestals conductively couple the input/output terminals of the associated chip to the underlying pathways. A **compression** spring is also provided for urging the chip towards the **substrate,** thereby coupling the conductive pads to the pathways through the resilient **compressible** pedestals.

Detailed Description Text - DETX (6):

In accordance with a second method of forming the pedestals 20 a coating of liquid polyimide is spun on the **substrate** 10 and cured. Photoresist is applied over the polyimide coating and exposed using a mask. Upon development the holes 14 in the polyimide coating are etched with a suitable etching fluid, the etching fluid reacting only with the polyimide and not the overlying photoresist. The overlying layer of photoresist is then removed by well known methods and a second application of photoresist is made. This second application of photoresist is made, in a manner similar to that used for delineating thick film **integrated circuits,** such that the holes 14 in the polyimide layer are filled with photoresist. Sufficient photoresist is applied such that a positive meniscus is formed in each of the holes. This second application of photoresist is accomplished by using a negative type of photoresist that is, a type that upon exposure to light and subsequent development remains intact. The layer of polyimide is next removed using a selective etchant which has no effect on the deposited photoresist pedestal 16. After deposition of the metalization upon the photoresist pedestal 16, the pedestal 16 is dissolved and removed by a suitable solvent, leaving the upstanding metallic **compressive** pedestals 20.

Current US Cross Reference Classification - CCXR (2):

257/E23.078

US-PAT-NO: 4902606

DOCUMENT-IDENTIFIER: US 4902606 A

TITLE: Compressive pedestal for microminiature connections

DATE-ISSUED: February 20, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Patraw; Nils E.	Redondo Beach	CA	N/A	N/A

US-CL-CURRENT: 430/314, 257/E21.511 , **257/E23.078** , 361/760 , 361/771 , 430/315 , 430/317 , 430/329 , 439/66 , 439/74

ABSTRACT:

Apparatus is disclosed for providing microelectronic, intra-chip and chip-to-chip interconnections in an ultra-dense **integrated circuit** configuration. **Compressive** pedestals 20 are used to form spring-loaded electrical and mechanical interconnections to conductive terminals on a chip interface mesa and chip assembly 28 in order to form a large multi-chip array 23 on an interconnection **substrate** 24. Methods are also disclosed for fabricating the **compressive** pedestals 20.

5 Claims, 8 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 2

---------- KWIC ---------

Abstract Text - ABTX (1):

Apparatus is disclosed for providing microelectronic, intra-chip and chip-to-chip interconnections in an ultra-dense **integrated circuit** configuration. **Compressive** pedestals 20 are used to form spring-loaded electrical and mechanical interconnections to conductive terminals on a chip interface mesa and chip assembly 28 in order to form a large multi-chip array 23 on an interconnection **substrate** 24. Methods are also disclosed for fabricating the **compressive** pedestals 20.

Detailed Description Text - DETX (5):

In accordance with a second method of forming the pedestals 20 a coating of liquid polyimide is spun on the **substrate** 10 and cured. Photoresist is applied over the polyimide coating and exposed using a mask. Upon development the holes 14 in the polyimide coating are etched with a suitable etching fluid, the etching fluid reacting only with the polyimide and not the overlying photoresist. The overlying layer of photoresist is then removed by well known methods and a second application of photoresist is made. This second application of photoresist is made, in a manner similar to that used for delineating thick film **integrated circuits**, such that the holes 14 in the polyimide layer are filled with photoresist. Sufficient photoresist is applied such that a positive meniscus is formed in each of the holes. This second application of photoresist is accomplished by using a negative type photoresist, that is, a type that upon exposure to light and subsequent

development remains intact. The layer of polyimide is next removed using a selective etchant which has no effect on the deposited photoresist pedestal 16. After deposition of the metalization upon the photoresist pedestal 16, the pedestal 16 is dissolved and removed by a suitable solvent, leaving the upstanding metallic **compressive** pedestals 20.

Current US Cross Reference Classification - CCXR (2):
257/E23.078

US-PAT-NO: 4813129

DOCUMENT-IDENTIFIER: US 4813129 A

TITLE: Interconnect structure for PC boards and integrated circuits

DATE-ISSUED: March 21, 1989

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Karnezos; Marcos	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 29/832, 257/E23.021 , **257/E23.078** , 361/774 , 439/74

ABSTRACT:

An interconnect structure for electrically coupling conductive paths on two adjacent, rigid **substrates,** such as PC boards or **IC** chips. The interconnect structure includes a number of buttons formed on a first **substrate,** and a number of contacts formed on a second **substrate**. The buttons are elastically deformable, and include a resilient core made from an organic material such as polyimide, and a metallic coating formed over the core. The two **substrates are compressed** between mounting plates such that the buttons are pressed against the contracts to make electrical contact.

3 Claims, 7 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

---------- KWIC ---------

Abstract Text - ABTX (1):
An interconnect structure for electrically coupling conductive paths on two adjacent, rigid **substrates,** such as PC boards or **IC** chips. The interconnect structure includes a number of buttons formed on a first **substrate,** and a number of contacts formed on a second **substrate**. The buttons are elastically deformable, and include a resilient core made from an organic material such as polyimide, and a metallic coating formed over the core. The two **substrates are compressed** between mounting plates such that the buttons are pressed against the contracts to make electrical contact.

Current US Cross Reference Classification - CCXR (2):
257/E23.078

US-PAT-NO: 4716049

DOCUMENT-IDENTIFIER: US 4716049 A

TITLE: Compressive pedestal for microminiature connections

DATE-ISSUED: December 29, 1987

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Patraw; Nils E.	Redondo Beach	CA	N/A	N/A

US-CL-CURRENT: 427/96, 216/18 , 257/E21.511 , **257/E23.078** , 427/259 , 427/265 , 427/266 , 438/613

ABSTRACT:

Apparatus is disclosed for providing microelectronic, intra-chip and chip-to-chip interconnections in an ultra-dense **integrated circuit** configuration. **Compressive** pedestals 20 are used to form spring-loaded electrical and mechanical interconnections to conductive terminals on a chip interface mesa and chip assembly 28 in order to form a large multi-chip array 23 on an interconnection **substrate** 24. Methods are also disclosed for fabricating the **compressive** pedestals 20.

2 Claims, 8 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 2

---------- KWIC ---------

Abstract Text - ABTX (1):
Apparatus is disclosed for providing microelectronic, intra-chip and chip-to-chip interconnections in an ultra-dense **integrated circuit** configuration. **Compressive** pedestals 20 are used to form spring-loaded electrical and mechanical interconnections to conductive terminals on a chip interface mesa and chip assembly 28 in order to form a large multi-chip array 23 on an interconnection **substrate** 24. Methods are also disclosed for fabricating the **compressive** pedestals 20.

Current US Cross Reference Classification - CCXR (3):
257/E23.078

PAT-NO: JP361198769A

DOCUMENT-IDENTIFIER: JP 61198769 A

TITLE: HYBRID INTEGRATED CIRCUIT

PUBN-DATE: September 3, 1986

INVENTOR-INFORMATION:
NAME
MURATA, MASATO

ASSIGNEE-INFORMATION:
NAME COUNTRY
NEC CORP N/A

APPL-NO: JP60039141

APPL-DATE: February 28, 1985

INT-CL (IPC): H01L025/04, H05K001/18

US-CL-CURRENT: 257/704, 257/E23.018 , **257/E23.078**

ABSTRACT:

PURPOSE: To reduce the size of the outer configuration, by arranging a chip carrier, on which a ROM is mounted, and conducting rubber in a recess in a ceramic case, fixing the chip carrier to the ceramic case itself, thereby omitting a fixed frame.

CONSTITUTION: As an electronic circuit **substrate** for a hybrid **integrated circuit,** a ceramic case 1, in which a ROM mounting recess 5 is formed, is used. In said case 1, electronic circuits other than the ROM are incorporated. The recess 5 is a region, in which conducting rubber 6 and a chip carrier 7, on which the ROM is mounted, are placed. The conducting rubber 6 is put beneath the chip carrier 7. The ROM and the rubber are fixed to the case 1 by a cap 8 for **compressing** the ROM and the conducting rubber. Outer leads 2 are taking out of the case 1. A ceramic cap 3 is connected to the case 1 by solder 4. The chip carrier function is provided in the ceramic case itself. The hybrid **integrated circuit** is made compact, and its price is made low.

PUB-NO: WO008704009A1

DOCUMENT-IDENTIFIER: WO 8704009 A1

TITLE: COMPRESSIVE PEDESTAL FOR MICROMINIATURE CONNECTIONS

PUBN-DATE: July 2, 1987

INVENTOR-INFORMATION:

NAME	COUNTRY
PATRAW, NILS E	US

ASSIGNEE-INFORMATION:

NAME	COUNTRY
HUGHES AIRCRAFT CO	US

APPL-NO: US08602509

APPL-DATE: November 24, 1986

PRIORITY-DATA: US81156085A (December 20, 1985)

INT-CL (IPC): H01L023/48, H01L023/32

EUR-CL (EPC): H01L021/48 ; H01L021/60, H01L023/48 , H05K003/40

US-CL-CURRENT: 257/724, 257/E21.511 , **257/E23.078**

ABSTRACT:

CHG DATE=19990617 STATUS=O>Apparatus for providing microelectronic, intra-chip and chip-to-chip interconnections in an ultra-dense **integrated circuit** configuration. **Compressive** pedestals (20) are used to form spring-loaded electrical and mechanical interconnections to conductive terminals on an chip interface mesa and chip assembly (28) in order to form a large multi-chip array (23) on an interconnection **substrate**(24). Methods are also disclosed for fabricating the **compressive** pedestals (20).

US-PAT-NO: 6590289

DOCUMENT-IDENTIFIER: US 6590289 B2

TITLE: Hexadecagonal routing

DATE-ISSUED: July 8, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Shively; John	Benicia	CA	N/A	N/A

US-CL-CURRENT: **257/758**, **257/760**

ABSTRACT:

Cell terminals in an integrated circuit is interconnected by using multiple layers of conductors that are routed both orthogonally and non-orthogonally to each other. Non-orthogonally routed conductors have slopes that are ratios of non-zero integers which approximate ceratin predetermined angles. The integers in the ratios are chosen from integers generated by sequence equations. The conductors are routed by following grid lines in a grid system comprising both orthogonal grid lines and non-orthogonal grid lines having slopes generated by the sequence equations. Ratios of integers are used to approximate certain angles so that the conductors would intersect the cell terminals located on the fundamental grid intersection points. The conductors in different metal layers form different angles with other conductors in other metal layers based on the slopes of the conductors.

66 Claims, 37 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 17

---------- KWIC ---------

Detailed Description Text - DETX (119):

Generally, the methods described herein with respect to **IC** design will be practiced with a general purpose computer, either with a single **processor** or multiple **processors**. The methods described herein will also be generally implemented in an ECAD system running on a general purpose computer. FIG. 28 is block diagram of a general purpose computer system, representing one of many suitable computer platforms for implementing the methods described above. FIG. 28 shows a general purpose computer system 650 in accordance with the present invention. As shown in FIG. 28, computer system 650 includes a central **processing** unit (**CPU**) 652, read-only memory (ROM) 654, random access memory (RAM) 656, expansion RAM 658, input/output (I/O) circuitry 660, **display** assembly 662, input device 664, and expansion **bus** 666. Computer system 650 may also optionally include a mass storage unit 668 such as a disk drive unit or nonvolatile memory such as flash memory and a real-time clock 670.

Current US Original Classification - CCOR (1):

257/758

Current US Cross Reference Classification - CCXR (1):
257/760

US-PAT-NO: 6480989

DOCUMENT-IDENTIFIER: US 6480989 B2

TITLE: Integrated circuit design incorporating a power mesh

DATE-ISSUED: November 12, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chan; Chun	San Jose	CA	N/A	N/A
Huang; Tammy	Fremont	CA	N/A	N/A
Liang; Mike	Milpitas	CA	N/A	N/A

US-CL-CURRENT: 716/8, **257/211** , **257/E23.153** , 716/11 , 716/14

ABSTRACT:

Provided is a technique for designing an integrated circuit die which includes a semiconductor layer, a primary metal layer, a horizontal metal layer and a vertical metal layer. Electronic components are laid out on the semiconductor layer, and a primary power distribution network for distributing power to the electronic components is laid out on the primary metal layer. Then, a uniform trunk width is calculated for all trunks in a power mesh based on a desired maximum voltage drop for the generated electronic component layout. Finally, horizontal power trunks are laid out on the horizontal metal layer and vertical power trunks are laid out on the vertical metal layer using the calculated uniform trunk width, so as to form the power mesh, and an electrical connection is specified between the power mesh and the primary power distribution network.

18 Claims, 10 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

---------- KWIC ---------

Detailed Description Text - DETX (51):

Generally, the methods described herein with respect to **IC** design will be practiced with a general purpose computer, either with a single **processor** or multiple **processors**. FIG. 9 is a block diagram of a general purpose computer system, representing one of many suitable computer platforms for implementing the methods described above. FIG. 9 shows a general purpose computer system 450 in accordance with the present invention. As shown in FIG. 9, computer system 450 includes a central **processing** unit (**CPU**) 452, read-only memory (ROM) 454, random access memory (RAM) 456, expansion RAM 458, input/output (I/O) circuitry 460, **display** assembly 462, input device 464, and expansion **bus** 466. Computer system 450 may also optionally include a mass storage unit 468 such as a disk drive unit or nonvolatile memory such as flash memory and a real-time clock 470.

Current US Cross Reference Classification - CCXR (1):

257/211

Current US Cross Reference Classification - CCXR (2):
257/E23.153

US-PAT-NO: 6457157

DOCUMENT-IDENTIFIER: US 6457157 B1

TITLE: I/O device layout during integrated circuit design

DATE-ISSUED: September 24, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Singh; Virinder	Fremont	CA	N/A	N/A
Liang; Mike	Milpitas	CA	N/A	N/A

US-CL-CURRENT: 716/2, **257/E23.079** , 438/14 , 716/10

ABSTRACT:

A method for laying out input/output (I/O) pairs, each including an I/O cell and a pad, on an integrated circuit die. Size information is obtained for each of a first I/O pair and a second I/O pair. A minimum pad spacing criterion is obtained which specifies a minimum distance between the pad in the first I/O pair and an element of the second I/O pair, and the first I/O pair and the second I/O pair are laid out so as to satisfy the minimum pad spacing criterion. Also provided is a method for laying out pads for input/output (I/O) cells on an integrated circuit die in which size information is obtained for each of a first I/O cell pad and a second I/O cell pad. A minimum pad spacing criterion is obtained, and the first I/O cell pad and the second I/O cell pad are laid out so as to satisfy the minimum pad spacing criterion.

12 Claims, 14 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 11

---------- KWIC ---------

Detailed Description Text - DETX (60):

Generally, the methods described herein with respect to **IC** design will be practiced with a general purpose computer, either with a single **processor** or multiple **processors**. FIG. 9 is block diagram of a general purpose computer system, representing one of many suitable computer platforms for implementing the methods described above. FIG. 9 shows a general purpose computer system 450 in accordance with the present invention. As shown in FIG. 9, computer system 450 includes a central **processing** unit (**CPU**) 452, read-only memory (ROM) 454, random access memory (RAM) 456, expansion RAM 458, input/output (I/O) circuitry 460, **display** assembly 462, input device 464, and expansion **bus** 466. Computer system 450 may also optionally include a mass storage unit 468 such as a disk drive unit or nonvolatile memory such as flash memory and a real-time clock 470.

Current US Cross Reference Classification - CCXR (1):

257/E23.079

US-PAT-NO: 6323559

DOCUMENT-IDENTIFIER: US 6323559 B1

TITLE: Hexagonal arrangements of bump pads in flip-chip integrated circuits

DATE-ISSUED: November 27, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chan; Chun	San Jose	CA	N/A	N/A
Liang; Mike	Milpitas	CA	N/A	N/A

US-CL-CURRENT: **257/778**, **257/786** , **257/E21.511** , **257/E23.021** , **257/E23.079**

ABSTRACT:

A flip-chip integrated circuit die includes a semiconductor substrate, electronic components implemented on the semiconductor substrate, several plural metal layers, wires routed between the electronic components on the metal layers, a top layer, and bump pads arranged in a hexagonal array on the top layer. According to another aspect, the invention is directed to flip-chip integrated circuit design, in which a circuit description is input and standardized cells which correspond to electronic components in the circuit description are obtained. The standardized cells are laid out on the surface of the die using a rectangular-based layout technique, and bump pads are laid out in a hexagonal array.

16 Claims, 16 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 13

---------- KWIC ---------

Detailed Description Text - DETX (45):

Generally, the methods described herein with respect to **IC** design will be practiced with a general purpose computer, either with a single **processor** or multiple **processors**. FIG. 15 is block diagram of a general purpose computer system, representing one of many suitable computer platforms for implementing the methods described above. FIG. 15 shows a general purpose computer system 450 in accordance with the present invention. As shown in FIG. 15, computer system 450 includes a central **processing** unit (**CPU**) 452, read-only memory (ROM) 454, random access memory (RAM) 456, expansion RAM 458, input/output (I/O) circuitry 460, **display** assembly 462, input device 464, and expansion **bus** 466. Computer system 450 may also optionally include a mass storage unit 468 such as a disk drive unit or nonvolatile memory such as flash memory and a real-time clock 470.

Current US Original Classification - CCOR (1):

257/778

Current US Cross Reference Classification - CCXR (1):

257/786

Current US Cross Reference Classification - CCXR (2):
257/E21.511

Current US Cross Reference Classification - CCXR (3):
257/E23.021

Current US Cross Reference Classification - CCXR (4):
257/E23.079

US-PAT-NO: 6225143

DOCUMENT-IDENTIFIER: US 6225143 B1

TITLE: Flip-chip integrated circuit routing to I/O devices

DATE-ISSUED: May 1, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rao; Ramoji Karumuri	Sunnyvale	CA	N/A	N/A
Liang; Mike	Milpitas	CA	N/A	N/A

US-CL-CURRENT: 438/106, **257/E23.079** , **257/E23.151** , **257/E23.152** , 438/107 , 438/108 , 438/613

ABSTRACT:

Tile-based routing between a bump pad and an input/output (I/O) device for implementation on a flip-chip integrated circuit (IC) die. A trace is routed between the bump pad and a position corresponding to a first I/O slot, the first I/O slot being at least partially occupied by the I/O device. A position is obtained for a device pad for the I/O device. The trace is then extended into an area corresponding to the position obtained for the device pad. It is a feature of this aspect of the invention that the trace extension extends the trace into a pad area for a second I/O slot, the second I/O slot being at least partially occupied by the I/O device. The invention also concerns a flip-chip integrated circuit (IC) die that includes a bump pad, an input/output (I/O) device, and a device pad electrically connected to the I/O device and disposed vertically adjacent to a portion of the I/O device. Also provided is an electrically conductive trace, including a first portion between the bump pad and a first position, the first position corresponding to a portion of the I/O device and being horizontally offset from the device pad, and also including a second portion between the first position and a second position corresponding to the device pad.

14 Claims, 11 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

---------- KWIC ---------

Detailed Description Text - DETX (43):

Generally, the methods described herein with respect to **IC** design will be practiced with a general purpose computer, either with a single **processor** or multiple **processors**. FIG. 10 is block diagram of a general purpose computer system, representing one of many suitable computer platforms for implementing the methods described above. FIG. 10 shows a general purpose computer system 450 in accordance with the present invention. As shown in FIG. 10, computer system 450 includes a central **processing** unit (**CPU**) 452, read-only memory (ROM) 454, random access memory (RAM) 456, expansion RAM 458, input/output (I/O) circuitry 460, **display** assembly 462, input device 464, and expansion **bus** 466. Computer system 450 may also optionally include a mass storage unit 468 such as a disk drive unit or nonvolatile memory such as flash memory and a real-time clock 470.

Current US Cross Reference Classification - CCXR (1):
257/E23.079

Current US Cross Reference Classification - CCXR (2):
257/E23.151

Current US Cross Reference Classification - CCXR (3):
257/E23.152

US-PAT-NO: 6057169

DOCUMENT-IDENTIFIER: US 6057169 A

TITLE: Method for I/O device layout during integrated circuit design

DATE-ISSUED: May 2, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Singh; Virinder	Fremont	CA	N/A	N/A
Liang; Mike	Milpitas	CA	N/A	N/A

US-CL-CURRENT: 438/14, **257/E23.079**

ABSTRACT:

A method for laying out input/output (I/O) pairs, each including an I/O cell and a pad, on an integrated circuit die. Size information is obtained for each of a first I/O pair and a second I/O pair. A minimum pad spacing criterion is obtained which specifies a minimum distance between the pad in the first I/O pair and an element of the second I/O pair, and the first I/O pair and the second I/O pair are laid out so as to satisfy the minimum pad spacing criterion. Also provided is a method for laying out pads for input/output (I/O) cells on an integrated circuit die in which size information is obtained for each of a first I/O cell pad and a second I/O cell pad. A minimum pad spacing criterion is obtained, and the first I/O cell pad and the second I/O cell pad are laid out so as to satisfy the minimum pad spacing criterion.

15 Claims, 14 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 11

---------- KWIC ---------

Detailed Description Text - DETX (62):

Generally, the methods described herein with respect to **IC** design will be practiced with a general purpose computer, either with a single **processor** or multiple **processors**. FIG. 9 is block diagram of a general purpose computer system, representing one of many suitable computer platforms for implementing the methods described above. FIG. 9 shows a general purpose computer system 450 in accordance with the present invention. As shown in FIG. 9, computer system 450 includes a central **processing** unit (**CPU**) 452, read-only memory (ROM) 454, random access memory (RAM) 456, expansion RAM 458, input/output (I/O) circuitry 460, **display** assembly 462, input device 464, and expansion **bus** 466. Computer system 450 may also optionally include a mass storage unit 468 such as a disk drive unit or nonvolatile memory such as flash memory and a real-time clock 470.

Current US Cross Reference Classification - CCXR (1):

257/E23.079

US-PAT-NO: 6031590

DOCUMENT-IDENTIFIER: US 6031590 A

TITLE: Structure and method of mounting driver IC using anisotropic conductive film in liquid crystal display device

DATE-ISSUED: February 29, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kim; Seong Jin	Seoul	N/A	N/A	KR

US-CL-CURRENT: 349/86, **257/E21.514** , 349/149 , 349/150

ABSTRACT:

A structure and method of mounting a driver IC using an anisotropic conductive film (ACF) in a liquid crystal display device is disclosed. ACFs are used in bonding a FPC (Flexible Printed Circuit) and in a COG (Chip on Glass) process at the same time. A film according to the present invention comprises a support film, a COG ACF adhered on one portion of the support film and a FPC ACF adhered on the other portion of the support film. Using the film disclosed in the present invention, the manufacturing process of the LCD panel becomes simpler and easier.

20 Claims, 35 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 13

---------- KWIC ---------

Brief Summary Text - BSTX (10):

There is an tape automated bonding(TAB) method for connecting the driver **IC** and terminal pad of the TFT arrays. The TAB method comprises an inner lead bonding(ILB) step and an outer lead bonding(OLB) step in which a film having conductive **bus** lines are connected with electrodes of the driver **IC**. The ILB step is to connect the electrode of driver **IC** to one side of a film lead with a bump, and the OLB step is to connect the terminal pad to the other side of the film lead. Referring to the FIG. 4, the TAB method is explained more detail. The bumps 41 are formed on the electrode 40 of the driver **IC**() (FIG. 4a). One side of a polyimide film 43 having conductive **bus** lines is mounted on the bumps 41(FIG. 4b). The bumps 41 and the film 43 are bonded by pressing with high temperature. Additionally, a protective resin 44 is coated on the connected part in order to enhance the resist against the moisture or stress (FIG. 4c). After that, the another side of the polyimide film is connected to the terminal pad of the **LCD** with an ACF using the similar **process**. Here, the conductive balls embedding in the polyimide film are connected to the lead line and the terminal pad. Consequently, in the TAB method, the driver **IC** is mounted out side of the **LCD** panel and the driver **IC** is connected to the terminal of the **LCD** using a film having conductive **bus** lines.

Brief Summary Text - BSTX (11):

Another method is a chip on glass(COG) method in which the driver **ICs** are manufactured on the glass of the **LCD** panel. In the COG method, the driver **ICs** are connected to the terminal pad with the bumps and the ACF film instead of using the polyimide film having conductive **bus** lines in TAB method. Therefore, the manufacturing **process** and the structure of the **LCD** is more simple. Furthermore, the screen area is larger in the same size of the glass panel.

Current US Cross Reference Classification - CCXR (1):
257/E21.514